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13. ABSTRACT *(Maximum 200 words)*

The study of the oxidation of Si-Ge alloys was successfully completed with the active collaboration of P.E. Thompson at the Naval Research Laboratory. A number of publications and talks resulted, in addition to two Ph.D. theses and one Master's degree. The work was accomplished as a three part study involving: **A)** A UHV, XPS and AES study of the very early stage of oxidation (<10Å). **B)** A low temperature conventional (fluorine added) oxidation. **C)** Electrical characterization by MOS technologies of implanted Ge. In Part A, oxidations were carried out under ultra high vacuum conditions in a Scientia ESCA300. Under these conditions, a systematic study of suboxides formed in situ at low temperatures was made. Attention was given to the conditions under which all SiO_2 or mixed SiO_2-GeO_2 resulted. In Part B, chemically enhanced oxidation (by fluorine) was undertaken in the temperature range of 600° - 800° C. The chemically enhanced oxides at 600°C were found to be mixed SiO_2-GeO_2 oxides by XPS and SIMS measurements. Electrical characterization of these oxides was also carried out. In Part C, work was performed on the role of Ge at the SiO_2 interface which resulted in obtaining understanding and quantification of implanted Ge and its role in hot carrier performance.

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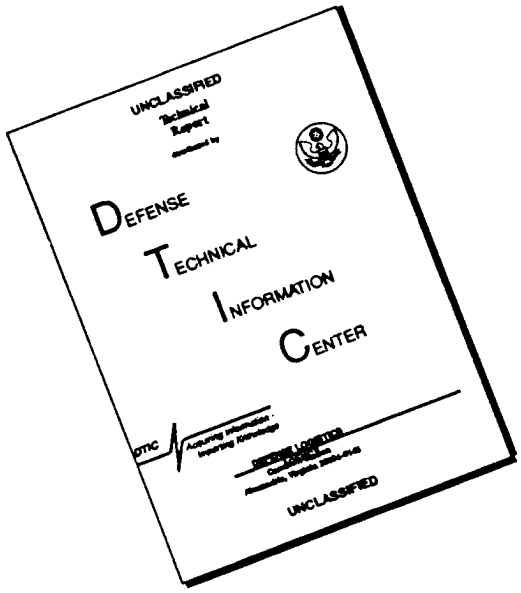

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RE: Final technical report for N00014-92-J-1308
Dr. Ralph J. Jaccodine, P.I.

Dear Dr. Goodman:

I am forwarding three copies of the final technical report for the referenced project.

If you have any questions or require additional information, please call me. I can be reached at (610) 758-3023 or via E-mail at MJH1@LEHIGH.EDU.

Sincerely,

Mary Jo Hill

Mary Jo Hill
Associate Director

MJH:gmw

Enclosures

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FINAL REPORT

"A Study of a New Approach to Low Temperature Oxidation of Ge-Si Alloy Material and its Characterization"

Dr. Ralph J. Jaccodine
Dr. Donald R. Young

Executive Summary

The study of the oxidation of Si-Ge alloys was successfully completed with the active collaboration of P.E. Thompson at the Naval Research Laboratory. A number of publications and talks resulted, in addition to two Ph.D. theses and one Master's degree.

The work was accomplished according to the plan as a three part study involving:

A) A UHV, XPS and AES study of the very early stage of oxidation (<10Å).
B) A low temperature conventional (fluorine added) oxidation.
C) Electrical characterization by MOS technologies of implanted Ge.

In Part A, oxidations were carried out under ultra high vacuum conditions in a Scientia ESCA300. A procedure for assuring surfaces were reproducibly clean was developed first. Study of initial monolayer coverage and subsequent conversion to oxide was instructive in tracking the very earliest stage of oxidation of the alloy. Under these conditions, a systematic study of suboxides formed in situ at low temperatures were made. Attention was given to the conditions under which all SiO_2 or mixed SiO_2-GeO_2 resulted.

In Part B, chemically enhanced oxidation (by fluorine) was undertaken in the temperature range of 600° - 800° C. The chemically enhanced oxides at 600° C were found to be mixed SiO_2-GeO_2 oxides by XPS and SIMS measurements. Electrical characterization of these oxides were carried out toward the end of the research period. The MOS measurements gave indication of real promise but further experiments were postponed in favor of finishing the theoretical work on a complete theory of the oxidation mechanism of these alloys. This theory seems to be confirmed by all the data we can find in the literature, and can be used to predict conditions for presence or absence of mixed oxides.

Results have been presented at the 42nd National Symposium of the American Vacuum Society (AVS) in Minneapolis (16-20 October, 1995); this work won Runner-Up honors for the 1995 Russell and Sigurd Varian Fellowship awarded by the AVS. Further

results were presented at the Spring Meeting of the Materials Research Society in San Francisco (8-12 April, 1996) in Symposium F on GeSi and Related Compounds. A detailed report of this research will be made in the Ph.D. dissertation of Stephen J. Kilpatrick, Lehigh University, to be completed on or about September, 1996.

In Part C, work was performed on the role of Ge at the SiO_2 interface which resulted in obtaining understanding and quantification of implanted Ge and its role in hot carrier performance. T.C. Lin's Ph.D. thesis explores the experiments and especially the hot carrier and other MOS techniques which led to the critical role of Ge in reducing hot carrier trapping with small effect on surface state density. This balance is an important finding in this study. The work of Mr. Krajci (M.S.) confirmed this finding and explored various options between implanted dose and energy and annealing conditions to optimize the Ge effect.

Part A.

In the study of the initial stages of oxidation, a variety of experiments were carried out in situ in the Scienta ESCA-300 ultra-high resolution x-ray photoelectron spectrometer. An electron beam heater was used to produce ultra-thin (<2 nm) oxides at 550-750°C and 1.5-3.0 x 10^{-6} Torr of O_2. A nichrome heater in a separate antechamber could achieve T<365°C at O_2 pressures from 2 x 10^{-5} to 760 Torr. Considerable attention was given to attaining a suitably cleaned surface prior to admitting oxygen. The samples as-received for MBE-grown SiGe had Ge-rich surface layers. After an RCA clean, the surface was returned to a bulk-like concentration, as evidenced by careful angle-resolved XPS. We found that two complete RCA cleaning cycles, with no water rinse following the HF etch step, separated by several hours for regrowing a native oxide, minimized the quantity of residual oxygen. For all samples (Ge contents of 1.8, 4.4, 8.5, and 16.8 atomic %) oxidized at the higher temperature/lower pressure conditions (550-750° C and 1.5-3.0 x 10^{-6} Torr), only SiO_2 was formed. Under the lower temperature/higher pressure conditions (<365° C and 2 x 10^{-5}-760 Torr), on the other hand, germanium oxidation was also observed. In all cases the relative suboxide intensities for the +1, +2, and +3 oxidation states were extracted by curve-fitting angle-resolved Si 2p and Ge 3d spectra. Si/Ge intensity ratios from a set of angle-resolved data were sometimes converted to concentration depth profiles of the surface region using the bussing and Holloway[1] algorithm. A final experiment (which has awaited equipment readiness) using a lecture bottle of O_2 mixed with 200 ppm NF_3 will create ultra-thin fluorinated oxides for comparison to the oxides grown in pure O_2 described above, and to those described below from our fluorinated quartz furnace.

Part B.

In the study of chemically enhanced oxidation in our quartz double-walled furnaces, a set of alloy samples with Ge contents as listed above were oxidized in 200 ppm NF_3 for different times between 15 and 150 minutes at temperatures ranging from 600-800° C. Oxide thicknesses ranging from 5-50 nm were measured by ellipsometry, profilometry, and SIMS (see Figure 1.)

SiGe layers oxidized in a fluorinated ambient at 700 and 800° C produced pure SiO_2, with no Ge detected by XPS in sensitive measurements down to a detectability limit of 45 ppm Ge. Interestingly, the oxidation kinetics for these films are accelerated by several times over results using dry O_2, and are also accelerated by a significant margin over pure Si oxidations in the same fluorinated ambient. This is in contrast to all reports in the literature on the kinetics of dry oxidation of SiGe, which state that Si and SiGe oxidize at the same rate[2]. Chemically enhanced oxidation of SiGe at 600° C, on the other hand, produced mixed oxides of SiO_2 and GeO_2, as evidenced by XPS and SIMS depth profiling. These mixed oxides increased considerably in thickness with increasing Ge content in the alloy. The pure SiO_2 oxides grown at higher temperatures did not show any thickness dependence on the alloy content. It is conjectured that these phenomena are indicators of the parallel influences which both Ge and F have on the point defect concentration on the semiconductor side of the oxidizing interface. For the case of the mixed oxides grown at 600° C, it appears that the influence of both Ge and F were observed, while in the case of the pure SiO_2 oxides grown at 700-800° C, it is likely that the F influence was dominant.

One of the mixed oxide (SiO_2 and /GeO_2) samples produced in a fluorinated ambient at 600° C is currently being metallized to form an MOS capacitor for electrical measurements. It is believed[3] that the Ge which is segregated at the oxidizing interface when pure SiO_2 is grown on SiGe causes unacceptable electrical properties for the oxide by forming interface traps. We are performing C-V and Q-V measurements on a mixed oxide sample to calculate the interface state trap density and comparing this with similar tests on MOS capacitors made from pure SiO_2 on SiGe. This will help to evaluate the potential usefulness of the mixed oxide on SiGe for electrical applications.

To aid in the theoretical understanding of these oxidation phenomena, both thermodynamic and kinetic calculations have been performed. Free energy calculations over a wide temperature range (550-1200 Kelvin) for all alloy contents (up to essentially pure Ge) have confirmed that both the equilibrium oxygen pressure at the oxidizing interface and the equilibrium mole fraction of GeO_2 in the oxide are always vanishingly small. Therefore all oxidation experiments on SiGe should produce pure SiO_2 according to thermodynamics.

A study of the oxidation kinetics, using a modified Deal-Grove approach[4] which adds a flux of silicon through the segregated Ge layer to the oxidizing interface, has yielded an insightful view over the entire range of practical experimental parameters (T, p_{02}, oxide thickness, and alloy composition.) The model predicts reasonable well whether an oxidation under a given set of parameters will produce pure SiO_2 or a mixed oxide (see Figure 2). This can be seen on a plot of the pressure-temperature parameter space which has been studied to date in this work and in the literature for the dry oxidation of SiGe (see Figure 3). The type of oxide achieved for each study is noted. A boundary is overlaid on the graph which separates pure SiO_2 formation from mixed oxide formation, as calculated from this modified Deal-Grove approach. This boundary is consistent with the experimental observations. Another prediction of the model is a rather strong effect from oxide thickness and alloy

composition on the oxide type formed. Under certain conditions a transition from one type to the other (e.g. from pure SiO_2 to mixed) will occur after a certain oxide thickness has been grown. Such complications have not been previously considered in the literature on SiGe oxidation. The model has also been extended to handle the effect of a fluorinated oxidizing ambient. The flux of oxidant arriving at the oxidizing interface as well as the reaction kinetics at the interface are strongly enhanced by the fluorine, and can be described by modified Deal-Grove rate constants, which have been measured by Kim et al.[5] in this laboratory for pure silicon. Finally, Wagner's classical theory[6] on binary alloy oxidation is presently being modified with a Deal-Grove rate equation and a concentration-dependent diffusivity to predict the silicon concentration gradient near the oxide, comparing this to the observed sharply defined Ge segregation layers which develop during pure SiO_2 formation.

Part C.

In 1990, K.K. Ng et al.[7] published a paper discussing the use of implanted germanium to reduce the hot electron injection from silicon to silicon dioxide in operating MOS transistors. They found a significant reduction in the deleterious effects of this injection but a very small degradation in the operating characteristics of the device. They suggested that implanted germanium scatters the hot carriers more effectively than the normal carriers. This observation intrigued us since this can easily be used on a semiconductor production line. It also posed an interesting scientific question concerning the scattering mechanism involved. As a result, we have had two graduate students investigate this further and the results of their work certainly supports the observations of Ng et. al[(1)]. This work has been supported by our ONR contract and we are certainly grateful for this support to make this work possible.

Most of our work has been done on MOS capacitor samples with germanium implanted with a peak concentration at the Si-SiO_2 interface. The implantation dose ranged from 10^{12} to $10^{15}/cm^2$. Ta-Cheng Lin in his Ph.D. work (supported by this contract) has observed a very large reduction in the hot electron injection as a result of this implantation. He has also observed that a large dose increases the interface state density and also increases the electron trapping rate in the oxide. These side effects limit the dosage that can be used. For a dosage of 10^{13} there was a negligible effect on the surface state density but there was a very large reduction in injection current. For dosages of 10^{14} or larger the interface state density did increase.

The energy of the implanted Ge was varied from 70 to 90 keV. These samples had an oxide thickness of 400Å. The 70 keV implantation resulted in the largest reduction in the injected current. The peak of the implantation was at the Si-SiO_2 interface so we conclude that this was the optimum location. These experiments should be extended to cover lower energies where the peak would be in the oxide.

It is well known that the injected electron current is much larger if the devices are operated at 77°K. This is due to the reduced scattering in the Si at these temperatures. It would be expected that the effect of the Ge implant would be even larger. This was found to

be the case. This is similar to the observation for metals that the decrease in the resistivity occurring at low temperatures is much larger for relatively pure metals than for impure metals.

Lin's work supported the observation of Ng et. al that Ge implantation had a negligible effect on the characteristics of operating transistors.

Lin further observed that the implantation dosage of 10^{13} did result in a significant increase in the electron trapping rate in the oxide which would partially counteract the beneficial effect of the germanium. The samples discussed above were made by implanting the germanium after the oxide was grown. Professor Ralph Jaccodine suggested to us that F.K. LeGoues had observed that the oxidation of Si-Ge alloys did not result in the presence of Ge in the oxide but the Ge piles up at the interface. As a result Lin made some samples with the Ge implanted before the oxidation. His results confirmed the results of Legoues since the result of this implantation did not increase the electron trapping rate in the oxide over that of the control sample (without germanium implantation.) A reduction of the injected electron current was also observed for these samples but it was not as large as for the implantation done after the oxide growth. Lin, however, did observe that there was a larger increase in the interface state density which is consistent with Legoues' observation that the germanium does pile up at the interface.

We are indebted to Charles Magee of Evans East, Plainsboro, NJ, who studied the germanium profiles using SIMMS techniques in samples related to our interests. For samples implanted before the oxidation there was a pileup of Ge at the Si-SiO_2 interface but a much larger concentration in the silicon than in the oxide. This was completely consistent with Lin's observation that there was no increase in charge trapping resulting from this implantation. For samples implanted after oxidation at the interface there was still a large buildup at the interface (probably due to the 1000°C heat treatment we always use to eliminate implantation damage.) However, the concentration of Ge in the oxide was at least an order of magnitude larger which was also consistent with Lin's observation of the enhanced electron trapping in the oxide. It is clear that the germanium prefers to be at the interface or in the silicon and will diffuse there if possible.

There had been a suggestion that the trapping resulting from the presence of Ge in the oxide was due to the fact that some of the Ge was partially oxidized. If that were the case then a short heat treatment in a oxidizing ambient might reduce the trapping. In addition we might expect that the prolonged heat treatment might gradually reduce the electron trapping due to the migration of Ge to the silicon. Martin Krajci conducted some experiments using heat treatments at 1000°C of 3 minutes and 30 minutes in an O_2 environment. He did not observe a reduction of electron trapping.

As a result of this work we conclude that the germanium does indeed significantly reduce the hot electron injection but it also increases the interface state density and also the electron trapping rate of the oxide. A reasonable compromise would be to use an

implantation dose of $10^{13}/cm^2$ implanted at the interface after the oxidation. This significantly reduces the hot electron injection but results in a minimal increase in electron trapping and interface state density.

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Publications/Presentations

"ARXPS Investigations of the Initial Oxidation Behavior of SiGe," S.J. Kilpatrick, R.J. Jaccodine, and P.E. Thompson, Forty-second National Symposium of the American Vacuum Society, Minneapolis, MN, October, 1995.

"The Effect of Fluorine on the Dry Oxidation Behavior of SiGe," S.J. Kilpatrick, R.J. Jaccodine, and P.E. Thompson, Spring Meeting of the Materials Research Society, San Francisco, CA, April, 1996.

"Characterization of Germanium Implanted MOS Devices," Ph.D. dissertation of Ta-Cheng Lin, Lehigh University, Bethlehem, PA, May, 1994.

"Optimization of Germanium Implanted MOS Devices For VLSI," Masters Thesis of Martin Krajci, Lehigh University, Bethlehem, PA, September, 1995.

"The Low Temperature Oxidation Behavior of SiGe Thin Films in a Fluorinated Ambient," S.J. Kilpatrick, Ph.D. Dissertation, Lehigh University, Bethlehem, PA, to be submitted.

Si vs. SiGe Oxidation Kinetics - 200 ppm NF_3

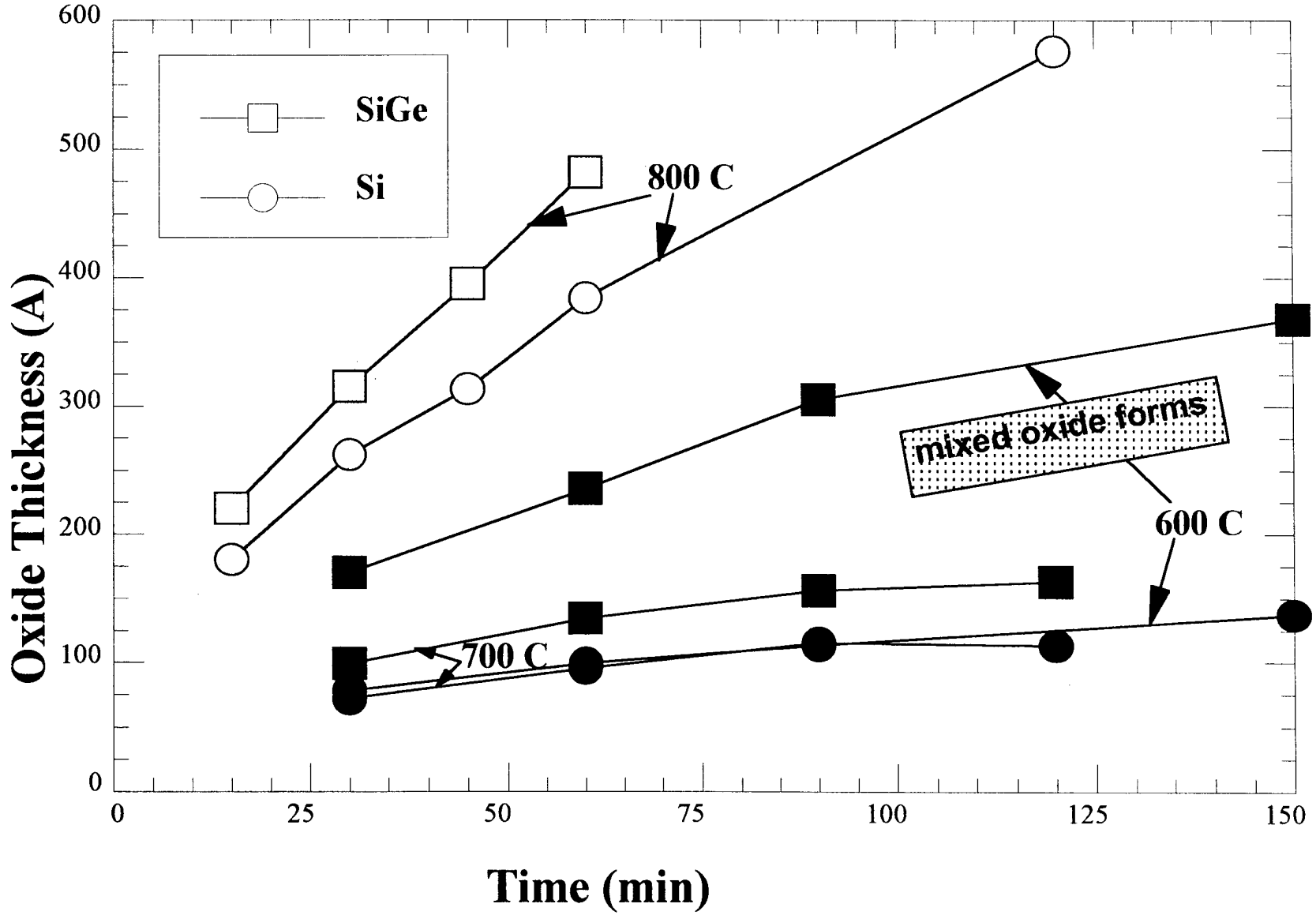

Figure 1

Change to Mixed Oxide Occurs During Growth

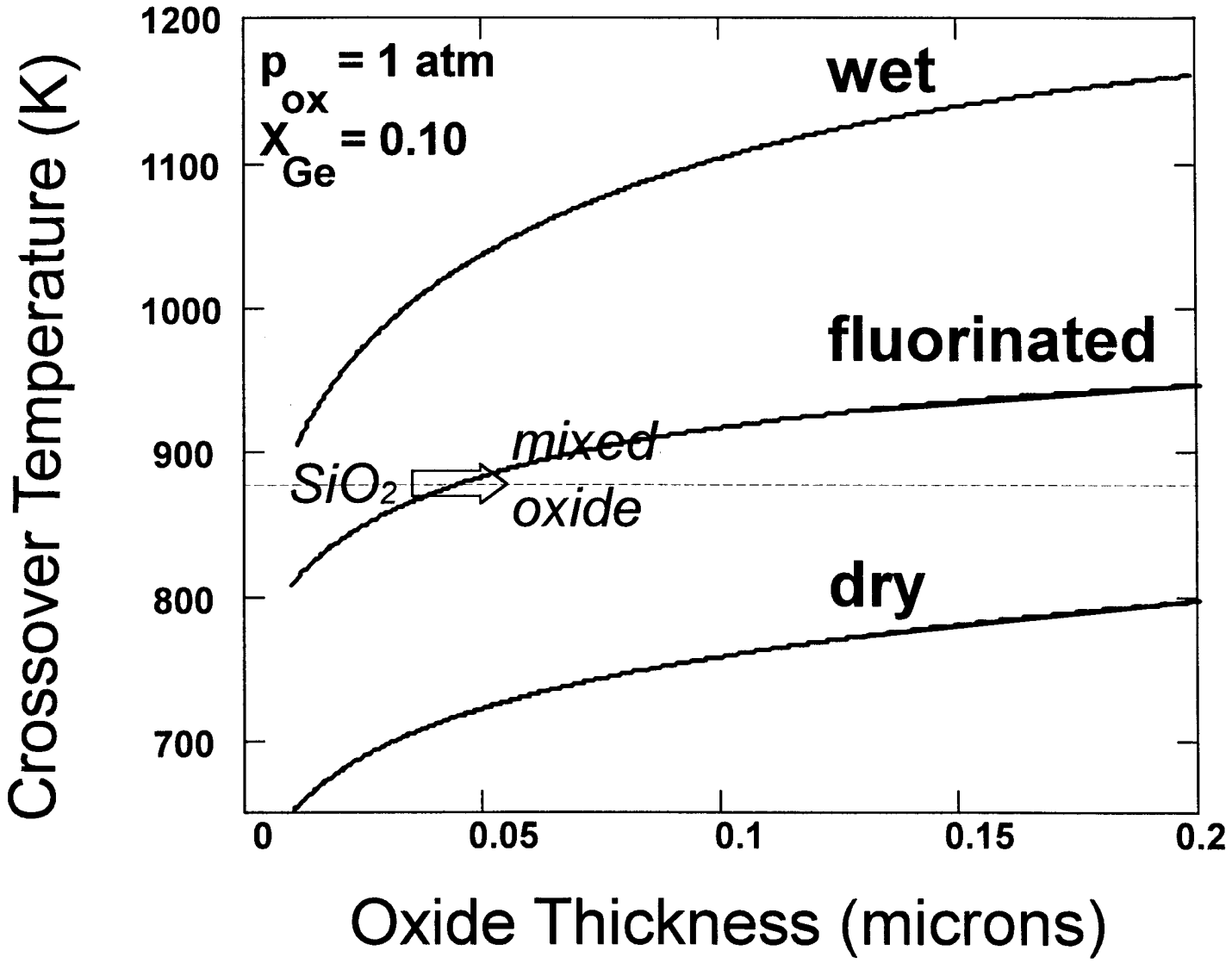

Figure 2

p-T Parameter Space for dry SiGe Oxidation

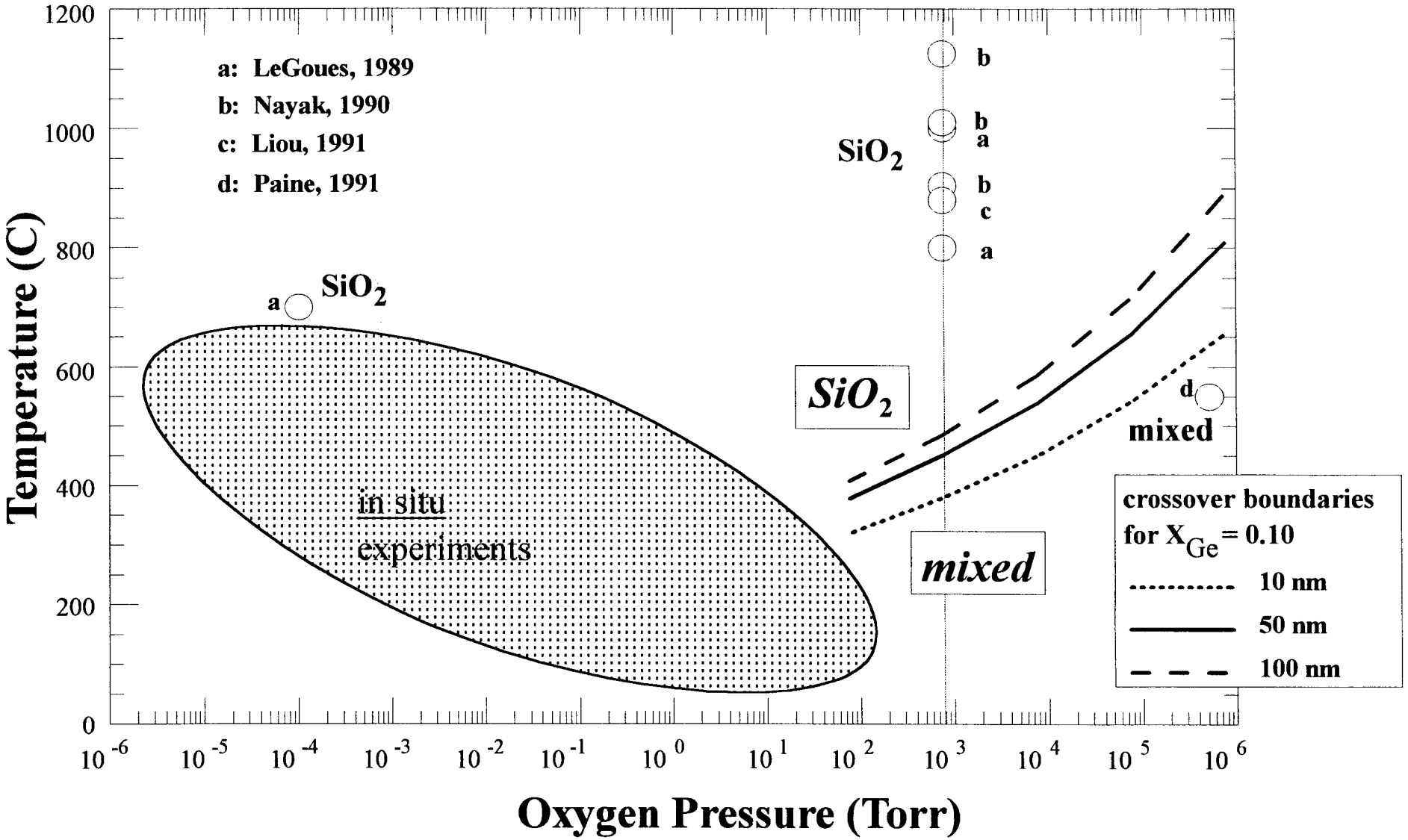

Figure 3

OPTIMIZATION OF GERMANIUM IMPLANTED MOS DEVICES FOR VLSI

by

Martin Krajci

A Thesis

Presented to the Graduate and Research Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

September 1995

Certificate of Approval

This thesis is accepted and approved in partial fulfilment of the requirements for the Master of Science.

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Date

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Thesis Advisor

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Co-Advisor

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Chairperson of Department

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I would like to express my gratitude to professors Ralph J. Jaccodine and Donald R. Young for their guidance, unlimited support, and encouragement during the course of this research. Also I am very grateful to Ta-Cheng Lin who started to work on this project during his studies at Lehigh University for his hours spent introducing me to the equipment in the laboratory, discussing his approaches and results with me, and guiding me through the initial stage of my research. I would like to thank Dr. Marvin White for giving us freedom to use his microelectronic laboratory. My thank you goes to Floyd Miller and especially Ray Filozof who has helped me enormously with my attempts to make my samples, and finally sacrificed his time to make the samples for me. I am indebted to Charles Magee of Evans East, Plainsboro, NJ, for conducting the SIMS profiles of my samples which added enormous value to this research. And finally, I would like to thank my fellow graduate students of electrical engineering and material science in Sherman Fairchild Laboratory, namely Humberto Raposo, Steve Killpatrick, Pam Yi-Pen Chi, Ansha Purwar, Su-Hong Lin, Ron Paulsen, Hari Sathianathan, Rob Klamka, David Fleischer, and Greg Sarcona for their friendly help and discussions.

We appreciate product and services provided by Virginia Semiconductor, Inc., Fredericksburg, VA, who supplied us with of Si wafers, and by Leonard J. Kroko, Tustin, CA, who performed Ge implantations.

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Table of Contents

List of Figures

Abstract

Hot electron effect which causes degradation of MOS devices becomes more of a concern when the devices become smaller, such as is the case in very large scale integration (VLSI). Hot electrons is a name assigned to electrons which gain enough energy in the channel to surmount the Si/SiO_2 barrier and enter the oxide. Among several possible approaches to reduce this effect, germanium doping seems to be very promising. It was believed that it is germanium in the region of Si/SiO_2 interface which acts as additional scattering mechanism and thus reduces the hot electron effect. On the other hand, past studies showed that Ge presence in the oxide also increases electron trapping rate in the oxide and surface state density. In this study, cases of pre- and post- Ge implantation oxidation as well as their combinations were analyzed on MOS capacitors. Avalanche injection was used to measure the susceptibility of a device to hot electron degradation, and the method was also used to measure electron trapping rate in the oxide. The CV and QV methods were used to estimate the interface trap density. SIMS was used to study Ge concentration profiles in Si/SiO_2 samples. The results showed that the hot electron effect reduction due to Ge does not depend on the presence of Ge in the Si/SiO_2 interface region but on the presence of Ge in the bulk oxide. The results confirmed belief that presence of Ge in the oxide increases the electron charge trapping rate and that presence of Ge in the region of Si/SiO_2 interface increases the interface trap density. SIMS results also showed that Ge atoms have a strong tendency to migrate from SiO_2 into the silicon, where they pile up near the interface.

Chapter 1: Introduction and Background

1.1. Introduction

With the advancement of the semiconductor technology which has currently progressed to very large scale integration (VLSI), development of smaller and faster devices has become the trend in the industry. These two factors go hand in hand, since the speed of a device is closely related to its physical size. Smaller devices have smaller gate and parasitic capacitances and thus can operate faster. Smaller devices allow also placing more devices into a single functional block and thus reducing the price. And with a smaller number of integrated circuit packages, system performance and reliability can be enhanced.

1.2. Scope of This Thesis

This chapter briefly introduces the subject of the hot electron effect and concerns associated with it. Common approaches to the hot electron effect reduction are also highlighted. The second chapter lists the methods utilized during this research and talks about the characteristic parameters which can be obtained by these methods. The third chapter presents the results of this research which are summarized in Chapter 4.

1.3. Hot Carrier Effect:

1.3.1. Introduction

As the MOS device becomes smaller, the electric field strength in the channel increases, and the electron's kinetic energy increases sufficiently to overcome the Si/SiO_2 potential barrier and cause appreciable electron emission into the oxide. These electrons with high kinetic energy are often referred to as "hot" electrons. It appears that this leads to generation of interface traps (surface states) and gives rise to a gate current. This is obviously a degradation of the device. The gate current I_g is commonly used as a measure of the device degradation.

As the electrons gain energy in the high field region flowing from source to drain, their energy reaches maximum around the drain and that is the region where most of the electrons surmount the potential barrier.

The source of hot electrons other than the channel current can also be the substrate current. Electrons either come from the bulk substrate region or are generated at the depletion region and drift towards the Si/SiO_2 interface. They gain energy from the high field in the depletion region. The hot electrons generated by high field in the substrate are referred to as the substrate hot electrons. The substrate hot electron effect is usually not significant in MOSFETS, unless the device has a heavily doped substrate and thus a much larger probability of a hot electron emission into the oxide, or the incident current is large (in cases such as elevated temperatures, forward biased junctions, or charge injection into the substrate from charge pumping of large MOS capacitors.)

1.3.2. Physical Model

The electrons gain energy from the electric field and accelerate towards the surface. At low fields their energy is too small to overcome the conduction band edge due to inelastic scattering. At about 20 kV/cm, optical phonon emission dominates the scattering process and the electrons' drift velocity saturates. At over 100 kV/cm, the electron starts to gain more energy than it can lose in the scattering and the electron-lattice equilibrium does not hold anymore.[1] After the electron's energy reaches a threshold value ϕ_I, the impact ionization becomes an important energy-loss mechanism. The combined mean free path can be expressed in terms of the contributions from optical phonon scattering (λ_p) and impact ionization (λ_I) as

$$\frac{1}{\lambda} = \frac{1}{\lambda_I} + \frac{1}{\lambda_p} \qquad (1.1)$$

The distance from the Schottky-lowered potential peak to the conduction band edge, X_c, represents most of the important parametric relationships. For example, increasing the substrate bias causes X_c to decrease. If we ignore tunneling and phonon absorption, for any $X<X_c$ the electrons have no chance to be emitted. If we assume that the most probable trajectory for an electron is the one with no scattering, the emission probability is

$$P = Ae^{\frac{-X_c}{\lambda}}, \qquad (1.2)$$

where A is a normalization constant, and λ is the combined mean free path of the mean free paths due to optical phonon scattering and impact ionization.

1.3.3. Static Degradation

There are three distinct regions for the carriers of the gate current. For low gate voltages ($V_G << V_D$), the gate current is hole-dominated. The main damage species in this region are interface traps, trapped holes, and neutral electron traps. Obviously, this damage is not immediately apparent, since the electron traps show no charge.[2]

In the region when $V_G = V_D/2$, the substrate current is maximum and both holes and electrons are injected into the gate while interface traps are generated. At higher gate voltages, the gate current is predominantly carried by the hot electrons which fill the neutral electron traps in the gate.[3]

1.3.4. Dynamic Degradation

As shown by Mistry *et al.*, at AC operation the resulting stress damage is a combination of factors from all three regions for the DC stress.[2] The proposed AC stress damage function consisting of the three damage mechanisms account for the so-called enhanced hot carrier degradation.

1.4. Hot Carrier Effect Reduction Techniques

1.4.1. Lightly Doped Drain (LDD)

Since the hot carrier effects are caused mainly by the high electric field near the drain, a common way to reduce it is by tailoring the doping profile in that region. The LDD (lightly doped drain) structure is currently the most often used technique. The idea is introducing a narrow self aligned lightly doped region in the area between the heavily doped drain and the channel area under the gate (Figure 1.1). In a conventional device, the electric field shows a strong peak in the region of the metallurgical junction and drops quickly to zero in the highly conductive n^+ region. In an LDD device, the peak of the electric field is extended and drops off slowly in the lightly doped region (Figure 1.2). Since the area of the graphs of electric fields for both conventional and LDD device has to be the same, the maximum field is reduced for a LDD structure. However, the introduction of a lightly doped region adds a series resistance between the channel and the drain. With scaling the channel to less than 0.5 microns, this resistance is not negligible. Additional problems were reported with the LDD structure as it is more susceptible to hot electron damage due to localized interface traps and trap charge located above the lightly doped drain.[4]

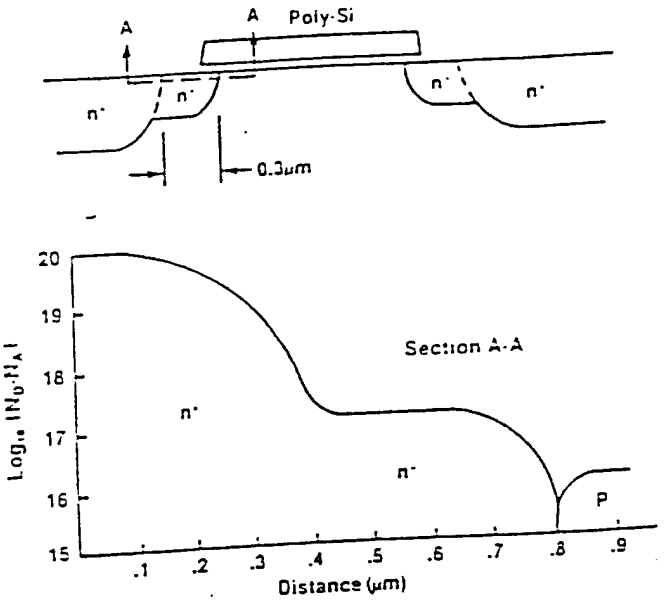

Figure 1.1 LDD Structure.

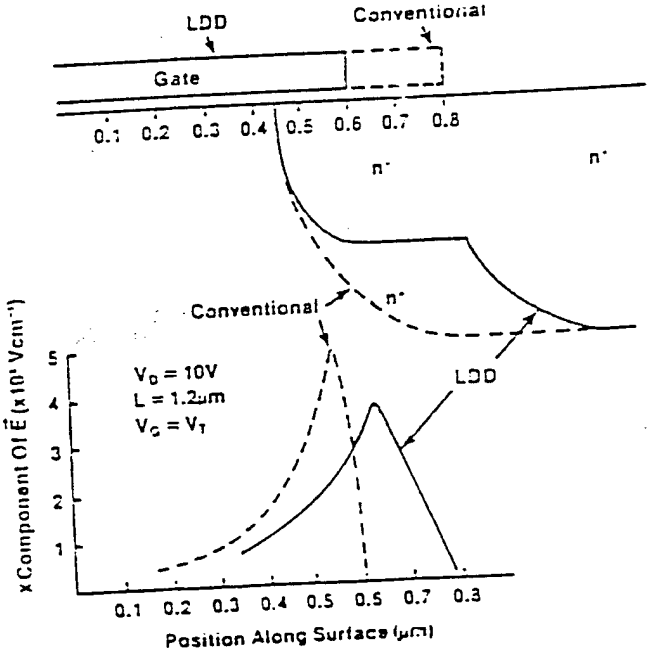

Figure 1.2. Magnitude of the electric field for the LDD and conventional devices at the Si/SiO_2 interface.

1.4.2. Reduction of operating voltage

Another approach to reducing the hot carrier effect is reducing the electric field by lowering the operating voltage. The standard has dropped from 5V to 3.3V, and recently a 2.5V standard was introduced to the state-of-the-art CMOS devices. However, the size of the gate tends to decrease much faster than the operating voltage, and thus the potential for device degradation due to the hot-carrier effects is still increasing. In addition, in BiCMOS circuits, the reduced V_{dd} required for MOSFETs is incompatible with bipolar devices.

1.4.3. Other Methods

One approach to reduce the degradation due to hot carriers is to decrease the charge trapping in the insulator.

Ma *et al.* found that adding fluorine to the oxide significantly reduces the hot-electron induced interface traps.[5] They claimed that the bond strain distribution near the Si-SiO_2 interface may be decreased by the presence of fluorine in the SiO_2.

Xie and Young found that fluorine implantation can reduce slow interface traps and eliminate the turn-around effect during avalanche injection.[6]

Kouvastos, *et al.*, studied incorporation and chemical bonding of fluorine introduced into SiO_2 thin films by NF_3-enhanced oxidation of Silicon.[7] They observed fluorine bonding in the oxide network in the area of oxidizing interface and passivating the interface trap centers.

It was also observed that the incorporation of nitrogen at Si-SiO_2 interface reduces the hot-carrier effect.[8] The so-called reoxidized nitride oxide (RNO) acts as a barrier for impurity penetration into the SiO_2 and reduces the interface trap generation. However, electron trapping is inherent in nitride oxide and reoxidation is necessary to reduce the hydrogen concentration. This reoxidation reduces the degradation of V_t and g_m.

1.4.4. Germanium doping:

A novel idea to suppress hot-electron effects was introduced by Ng *et al.* The technique is based on introduction of neutral germanium atoms in the channel region.[9] Ge atoms, being neutral, do not change the field and thus do not change significantly the carrier mobility. However, they can introduce the additional scattering mechanisms for the "lucky" hot carriers. They explain it by the fact that the Ge atoms are larger and thus introduce the added scattering. The added scattering is often attributed also to the fact that SiGe has smaller energy bandgap than Si. Conceptually, the mobility of the channel carriers is largely determined from surface scattering whose mean free path is on the order of the inversion-layer thickness. A small number of "lucky" hot carriers escape some of these scattering events and thus have a longer mean-free path. The intention here is to introduce an additional scattering mechanism with a mean free path value larger than the one seen by the majority of the channel carriers. Then the MOSFET channel current is not modified, but the the "lucky" hot carriers lose energy due to the added scattering.

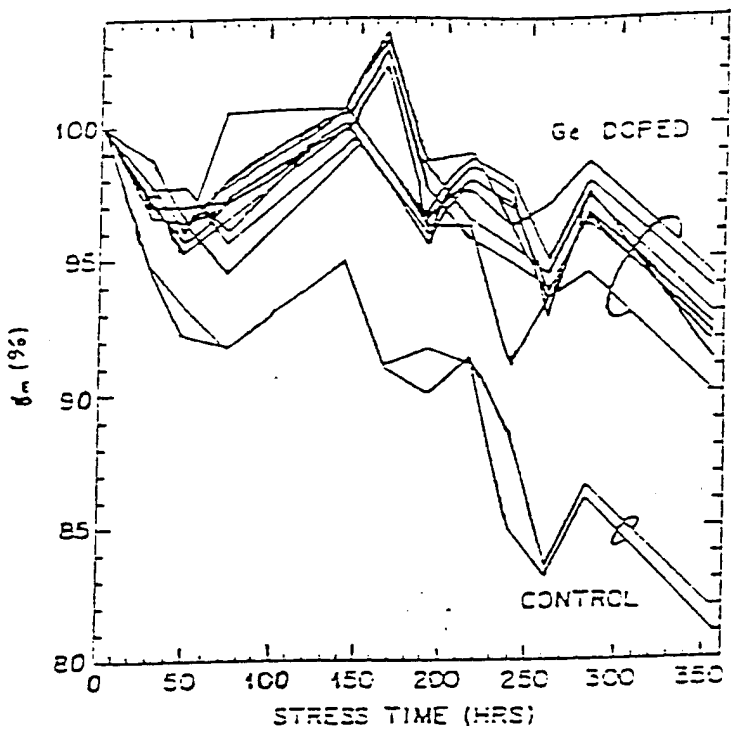

Figure 1.3 Transconductance g_m in the triode region relative to the initial value as a function of stress and time for the control devices and Ge-doped structures.

They showed that by introducing Ge impurities in the channel region of a Si MOSFET, the degradation rate under voltage stress is significantly reduced without modifying the initial characteristics (Figure 1.3).

Lin elaborated on this idea and showed that the population of hot carriers in Si is strongly reduced by the Ge implantation.[10] In his interface trap density study he found that when the Ge dose is equal to 10^{14} cm^{-2} the interface trap density increases. To obtain the maximum hot carrier reduction without increasing the interface trap density, the

implantation dose should be less than 10^{14} cm^{-2}. He also studied the effect of the location of the peak of the Ge implantation and found the optimal location at the Si-SiO_2 interface (Figs. 1.4, 1.5).

Lin also showed, in his charge trapping study, that the trapping rate of the Ge implanted samples in the SiO_2 increases with the Ge dose. His explanation for this fact was that the increase in trapping rate results from the formation of GeO, since the Ge bonds that are not involved in the network formation act as very efficient electron traps. In a modified process, Lin implanted Ge before oxidation. His results showed that even though the trapping rate was reduced (Fig. 1.6), the hot-carrier reduction effect also diminished (Fig. 1.7), and the interface trap density increased.[2]

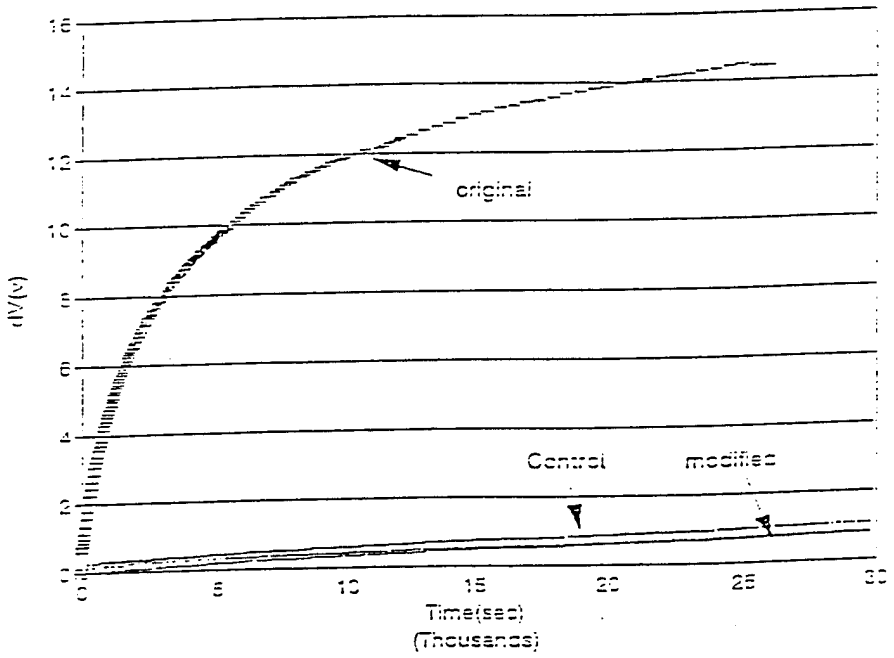

Figure 1.4 Avalanche injection current versus gate voltage curves show significant hot electron effect reduction for the case when germanium was implanted into the SiO_2. This reduction is weak for the case when the sample was oxidized only after germanium was already implanted in the silicon.

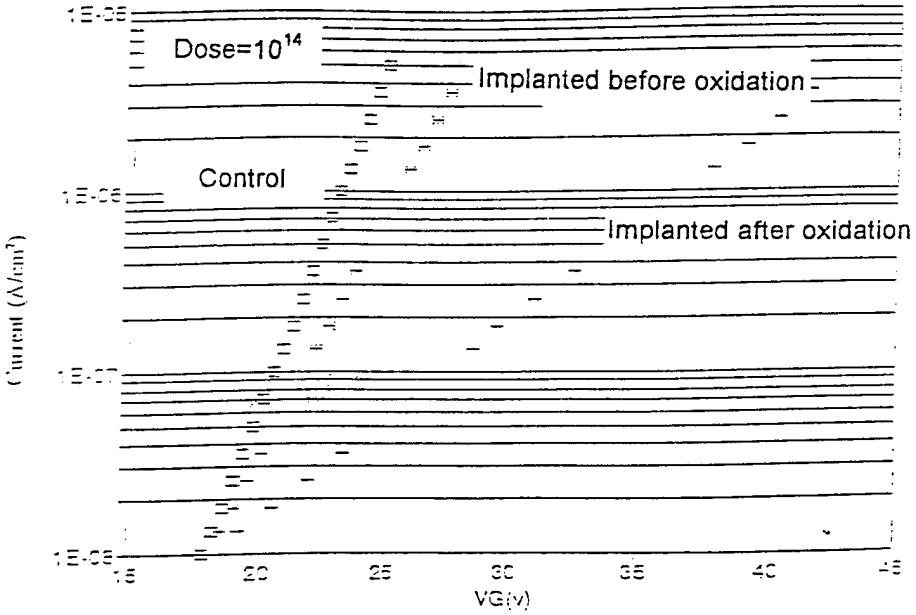

Figure 1.5 Flatband voltage shift versus time curves show significant increase in electron trapping rate for the case when germanium was implanted into the SiO_2. The electron trapping rate remains low for the case when the sample was oxidized only after germanium was already implanted in the silicon.

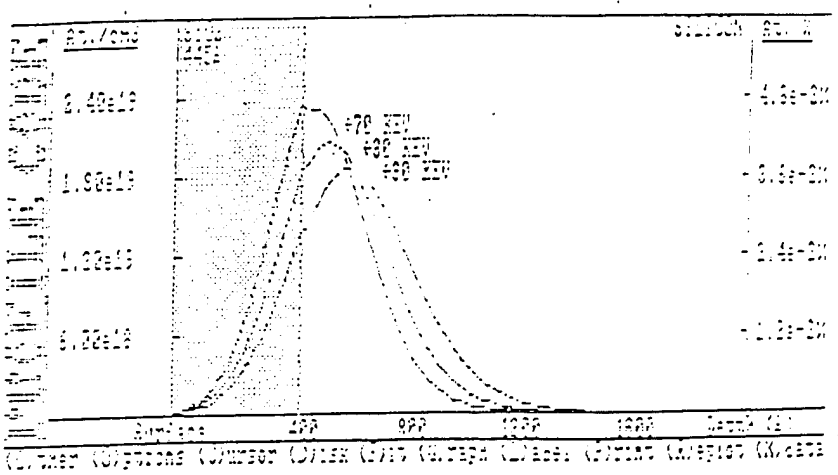

Figure 1.6 Simulated Ge profiles for various implantation energies in SiO_2/Si.

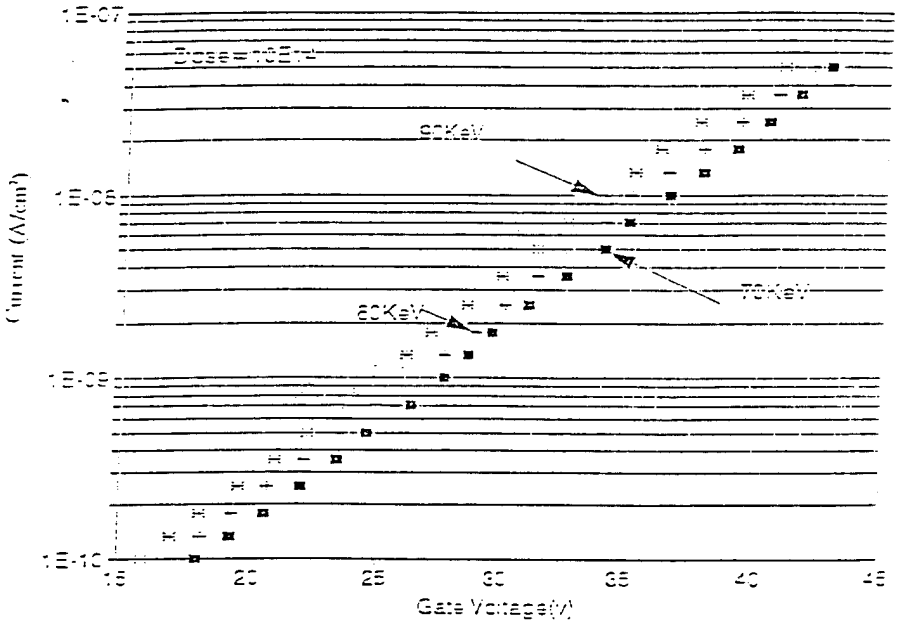

Figure 1.7 Avalanche injection current versus gate voltage curves show better hot-electron effect reduction if the peak of implantation is moved closer to the Si/SiO_2 interface.

Chapter 2: Experimental Procedures and Analytical Techniques.

2.1. MOS Capacitor:

MOS Capacitor is the simplest MOS structure and the structural basis for all MOS devices.

2.1.1. Manufacturing MOS capacitors:

The MOS capacitors for this set of experiments are manufactured on boron-doped p-type Si wafers. After the initial oxide was thermally grown on them, the wafers were sent for Ge implantation. Then if additional oxidation was required, it was performed. The wafers were then placed in an evaporator for evaporation of aluminum. The capacitors were then defined using a photolithography process, and the unwanted aluminum etched. Finally, the samples were thermally annealed.

2.2. High Frequency CV Measurement

The high frequency Capacitance-Voltage technique is a very useful method of analysis of MOS capacitors. The capacitance is defined *as* $C=dQ/dV$. It is a change of charge due to a change of voltage. The high frequency curve is obtained when the inversion charge is unable to follow the ac voltage. However, the dc bias should not be changed rapidly with insufficient time for inversion charge generation because then a deep depletion curve results.

The high frequency semiconductor capacitance in inversion is difficult to calculate exactly, even though exact expressions do exist. The following expression is accurate to 0.02% in strong inversion:

$$C_{S,HF} = \sqrt{\frac{q^2 K_S \varepsilon_0 N_A}{2kT\left\{2|U_F| - 1 + \ln\left[1.15\left(|U_F| - 1\right)\right]\right\}}}, \qquad (2.1)$$

where $U_F = \frac{q\phi_F}{kT}$ is the Fermi potential. The flatband voltage is determined by the metal-semiconductor workfunction difference ϕ_{MS} and the various oxide charges through the equation

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{\gamma Q_m}{C_{ox}} - \frac{\gamma Q_{ot}}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}}, \qquad (2.2)$$

where Q_f is the fixed oxide charge, Q_m mobile oxide charge, Q_{ot} is charge trapped in the oxide, and Q_{it} is the interface state charge. ϕ_{MS} is the metal-semiconductor workfunction, and ϕ_s is the semiconductor workfunction.

The effect of oxide charges on the flatband voltage shift is the greatest when the charge is near the Si-SiO_2 interface since it images all of its charge in the semiconductor. When the charge is located at the gate-oxide interface, it images all of its charge in the gate and has no effect on the flatband voltage. To account for the possible charge distribution throughout the oxide, a factor γ is introduced, which is defined by

$$\gamma = \frac{\int_0^{W_{ox}} (x/W_{ox})\rho(x)dx}{\int_0^{W_{ox}} \rho(x)dx}, \qquad (2.3)$$

where $\rho(x)$ is the oxide trapped or mobile charge per unit volume, and x is defined as the distance from the oxide-gate interface (i. e. $x=W_{ox}$ at the oxide-semiconductor interface.) The various charges and the workfunction difference result usually in a shift of the CV curve. The voltage shift can be theoretically evaluated at any capacitance; however it is usually measured at the so-called flatband capacitance C_{FB}., which is defined as the capacitance at the flatband voltage V_{FB}.. The flatband voltage is zero for an ideal high frequency CV curve (i. e. Q_{it} is assumed to be zero.)[11]

In the high frequency CV curve measurement for this experiment, a DC voltage is swept over a certain range with a 1 MHz small signal superimposed on it. Capacitance of the sample is measured at each point of the sweep and the CV curve is constructed. In our setup, we used a commercially available device 401 CV Plotter by Princeton Applied Research which incorporates all the features necessary to obtain a high frequency CV curve and provides a DC analog voltage outputs linearly proportional to the applied DC voltage and the corresponding measured capacitance, both as a function of time. These voltages were then sampled and recorded by a personal computer using a Keithley DAS-1600 data acquisition card.

2.2.1. Parameters extracted from a high frequency CV curve

The experimental CV curve can be compared with an ideal CV curve and the following parameters can be extracted.

The *fixed oxide charges* (Q_f) cause rigid shifts in the flatband voltage which can be used to determine the charge density.

The energy states of the *interface traps* are distributed throughout the silicon bandgap. As the gate voltage is swept from accumulation from inversion, it moves the Fermi level, it has to charge both the traps in the interface and in the semiconductor (since $Q_G=Q_S+Q_{it}$), assuming zero oxide charges, and therefore the charge state changes. As a result, the magnitude of the interface traps charge depends on the gate voltage. The presence of the interface traps will result in stretching out the CV curve.[2]

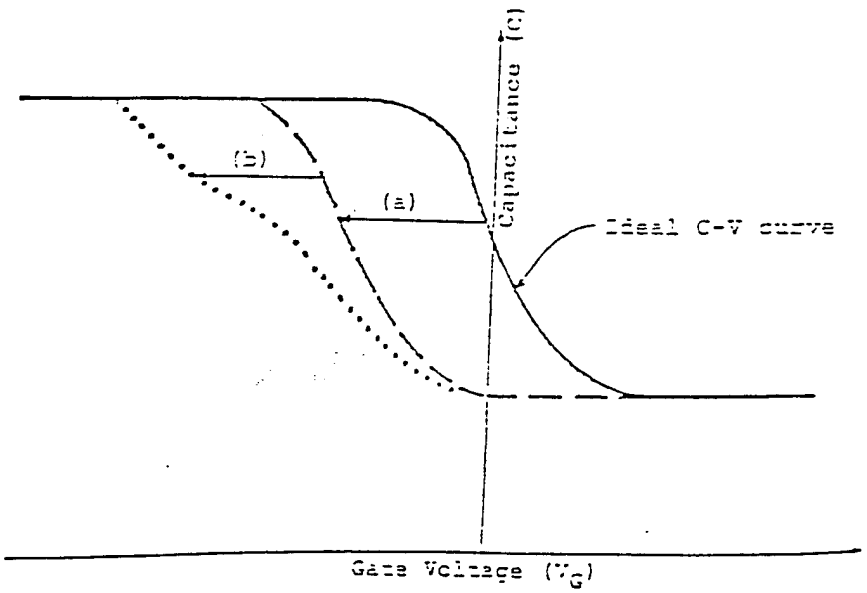

Figure 2.1 High frequency C-V curve for a p-type substrate MOS capacitor. (a) Rigid shift. (b) Stretch-out effect.

2.3. The QV Method

In this method (refer to Figure 2.2), a bias-independent reference capacitor C_i is connected in series with the MOS capacitor. Parasitic capacitances are usually so small that they can be neglected. A bias V_a is applied across C_i in series with the MOS capacitor. After steady state is reached, Va and the voltage across C_i, V_i is measured. The bias across the series is slowly varied point-by-point so that the MOS capacitor is always in a thermal equilibrium. From the known values,

$$V_G = V_a - V_i. \qquad (2.4)$$

Then the measured charge on the MOS capacitor is

$$\Delta Q_G = C_i V_i \qquad (2.5)$$

By varying the applied bias V_a the charge ΔQ_G can be obtained as a function of V_G. Next, the surface potential Ψ_σ is determined, as a difference between V_G and the voltage drop across the oxide, which is equal to Q_G/C_{ox}.[12]

$$\Psi_s = V_G - \frac{Q_G}{C_{ox}} - \Psi_0, \qquad (2.6)$$

where Ψ_0 is the surface potential for V_G=0.

To determine Ψ_0, we assume that in accumulation the interface potential is at the edge of the silicon valence band (for p-type silicon) and for strong inversion it is at the edge of the silicon conduction band. The mid point between the measured values is taken for the mid gap point. This mid gap potential is then used as a reference point.

The obtained curve is then compared with a theoretical curve obtained by Kingston-Neustadter theory[2], and the shift of V_G between the experimental and theoretical curves is determined. This difference is caused by the interface trap charge, fixed charge in the oxide, and the work function difference between metal and SiO_2:

$$C_{ox}\Delta V_G = \Delta Q = Q_f + Q_{it} + \omega, \qquad (2.7)$$

where Q_f is the fixed charge in the oxide, Q_{it} is the interface trap charge, and ω is a constant associated with the work function difference. Since only the interface trap charge Q_{it} is dependent on the gate voltage V_G, the derivative with respect to Ψ_s, will be

$$\frac{\partial(\Delta Q)}{\partial \Psi_s} = \frac{\partial Q_{it}}{\partial \Psi_s}. \qquad (2.8)$$

The interface trap density is then given by an equation

$$D_{it} = \frac{1}{qA} \times \frac{\partial Q_{it}}{\partial \Psi_s}, \qquad (2.9)$$

where A is the area of the gate, and q is an electron charge.[2]

2.3.1. Experimental Setup:

The laboratory setup for the QV measurements is based on the basic QV technique. A voltage independent precision capacitor C_i is connected in series with the MOS capacitor. The measurement procedure is controlled by a personal computer. A 12-bit digital-to-analog converter generates the voltage in the range of ±5V. This voltage is buffered and amplified to obtain the value of V_a in the range of ±10V. The voltage V_i across the bias-independent capacitor C_i is measured by a Keithley 616 electrometer which has an input impedance greater than 2×10^{14} Ω. The analog output of the electrometer is brought to a 16-bit analog-to-digital converter which supplies the value of C_i to the personal computer. This voltage can be measured with a 0.3 mV accuracy. The software written by Ta-Cheng Lin[2] controls the procedure and calculates the results.

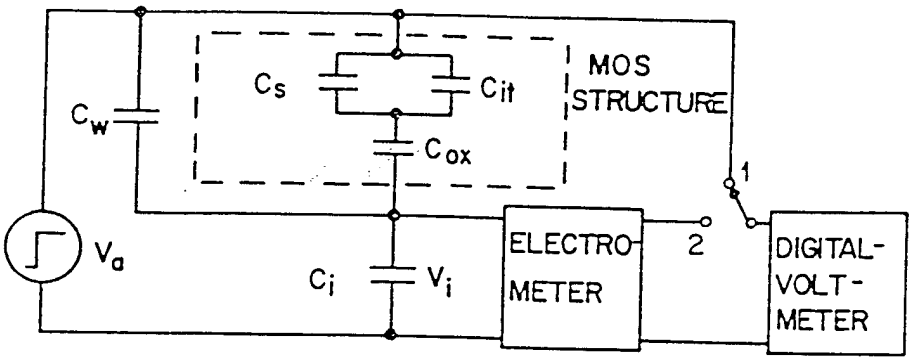

Figure 2.2 Basic QV measurement setup. In this analysis, the capacitance due to interface traps C_{it} is neglected. In our measurement, the voltage V_a is supplied and electrometer measured voltage read by a computer controlled system.

2.4. Avalanche Injection

In avalanche injection, carriers are accelerated by the applied electric field. When the field at the silicon surface reaches the avalanche breakdown value, carriers generated at the surface depletion layer are accelerated to energy high enough so that impact ionization occurs. Some of the electrons have enough energy to surmount the interfacial energy barrier and enter the SiO_2.

2.4.1. Physical Description

The first step towards avalanche injection is producing sufficient band bending to produce an avalanche plasma at the silicon surface of a MOS capacitor. To produce such band bending, the silicon must be driven to deep depletion. Deep depletion is produced by applying a large amplitude ac signal of a high enough frequency for minority carriers to follow. The band bending increases with increasing ac voltage, until the field at the silicon surface becomes high enough for avalanche breakdown. The avalanche plasma is generated once per cycle. A small number of the electrons have sufficient energy to surmount the interface energy barrier. In the oxide, these electrons tend to drift towards the gate driven by the electric field across the oxide, and through the external circuit which can detect a current pulse at each cycle. The injected current has to be emission limited, since significant trapping in the oxide may occur which causes a decrease in the injection current when the electron traps are filled and the field in the oxide is altered.

Figure 2.3 (a) illustrates one cycle of the oxide field produced by the external dc drive. At time t=0, the bands are assumed to be flat. The bands continue to bend as the

field increases until deep depletion is reached at time t_1. The avalanche breakdown begins at the beginning of the time interval t_A. The breakdown is initiated by thermally generated carriers and occurs at the silicon surface. Figure 2.2 (d) shows band bending at some time during the avalanche breakdown period t_A, as electrons are excited from the valence band to the conduction band of the silicon by impact ionization. Most electrons have energies below the interfacial barrier height, and these form an inversion layer. However, some have energies higher than the barrier height, and those do not get scattered back into silicon but enter the oxide where they drift towards the gate. The avalanche injection is terminated when the oxide field passes its peak value.

During the remainder of the cycle (Figure 2.3), when the band bending decreases back towards the flatband condition, electrons in the inversion layer generated during the interval t_A are injected back into silicon where they recombine. During the negative peak of the cycle, when accumulation occurs, no carriers are injected into the oxide since the holes at silicon surface see a barrier greater than 4 eV. Thus, the injected gate current is unidirectional.

The avalanche injection method can be used as a measure of the hot electron effect in MOS capacitors. Even though quantitative analysis of the energy distribution of hot electrons is rather complicated, the curves of injection current density versus gate voltage amplitude can be used to comparatively evaluate the magnitude the hot electron effect.

The avalanche injection method can also be used to obtain parameters related to oxide charge trapping. The method consists in applying a signal generating avalanche current through the MOS capacitor. The electrons in the oxide fill up the electron traps

and thus cause a flatband voltage shift. The value of this voltage shift reflects the trap density per unit area in the oxide.

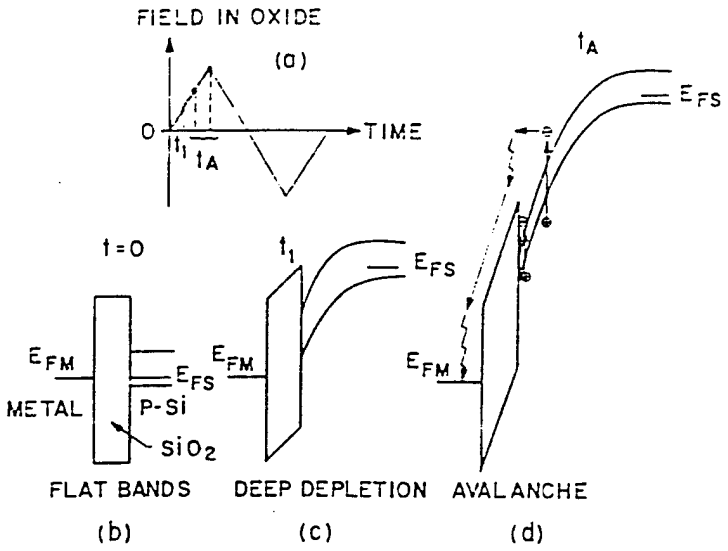

Figure 2.3 Diagram illustrating the principle of avalanche injection of electrons: (a) One cycle of the oxide field is produced by an external saw-tooth generator. (b), (c), and (d) show band bending in the silicon at various times during the cycle.

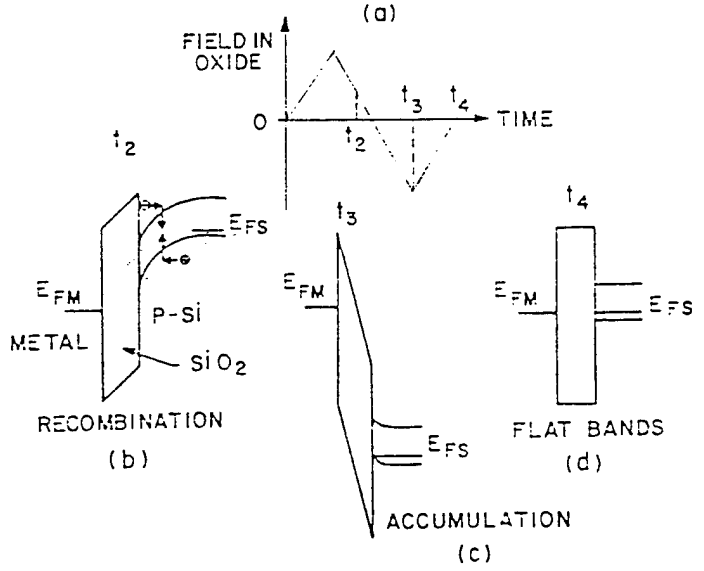

Figure 2.4 Diagram illustrating band bending in the silicon at various times after the avalanche portion of the cycle has been completed.

2.4.2. Experimental Setup

The experimental setup for the avalanche injection was designed by D.R. Young[13]. During the whole process of avalanche charge injection, the average DC current is kept at a constant value. A 150 kHz sawtooth signal is generated by an HP 3310A function generator as the applied source for avalanche injection. The automatic data acquisition system monitors the flatband voltage as a function of time or charge fluence.

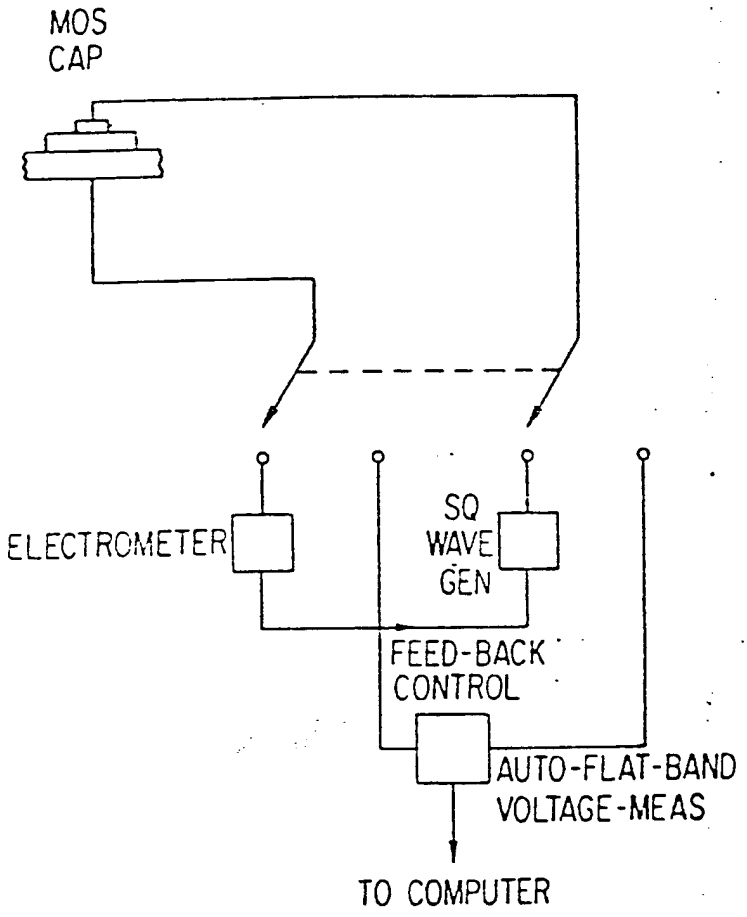

Figure 2.5 Schematic drawing of apparatus used for avalanche injection.

2.5. Secondary Ion Mass Spectrometry

Secondary ion mass spectrometry (SIMS) is a powerful technique for analysis of impurities in solids. The technique relies on removal of material from a solid and analysis of the sputtered ionized species. Most of the sputtered atoms are neutral and cannot be analyzed. Only the ionized atoms can be analyzed in an energy filter and a mass spectrometer.

A SIMS doping concentration is produced by sputtering the sample and monitoring the secondary ion signal of a given element as a function of time. The "ion signal versus time" can be converted to a dopant concentration profile. The time axis is converted to a depth axis by measuring the depth of the crater at the end of the measurement. The crater depth measurement has to be done after each measurement since the sputter rate varies with spot focus and ion current. The secondary ion signal is converted to impurity concentration through standards of known dopant profile. To determine an unknown impurity profile in a sample, the secondary ion signal is calibrated by an implanted sample with a known impurity concentration profile.

Sputtering is a process in which incident ions lose their energy mainly by momentum transfer as they come to rest within the solid. In the process they displace atoms within the sample. Sputtering takes place when atoms near the surface receive sufficient energy from the incident ions to be ejected from the sample. The primary ion loses its energy in the process and comes to rest several tens to hundreds of Å below the sample surface.

SIMS determines the total impurity concentration, not the electrically active impurity concentration. Therefore the results obtained through SIMS may be significantly different from the results obtained in electrical characterization since the sample may contain ions which are not yet electrically activated.

The strength of SIMS lies in its accepted use of dopant profiling. It measures the dopant profile, not the carrier profile, and therefore it can be used for implanted samples before any activation anneals. SIMS also has a high spatial resolution.[11]

We are indebted to Dr. Charles Magee and Ephraim Botnick of Evans East, Plainsboro, NJ, for performing the SIMS depth profiles. Our samples were depth-profiled using instrument 6600 for ^{70}Ge ions. The primary bombarding species used were Ox+ under a 60° angle. The primary ion energy was 3 keV, beam current 100 nA, raster size 300×300 μm, detected area 120×120 μm, with electron beam compensation on. The depth scale was established by measuring the depth of each crater sputtered into the samples by a calibrated profilometer. The overall accuracy of the profiles can be expected in the 15 to 20 % range.

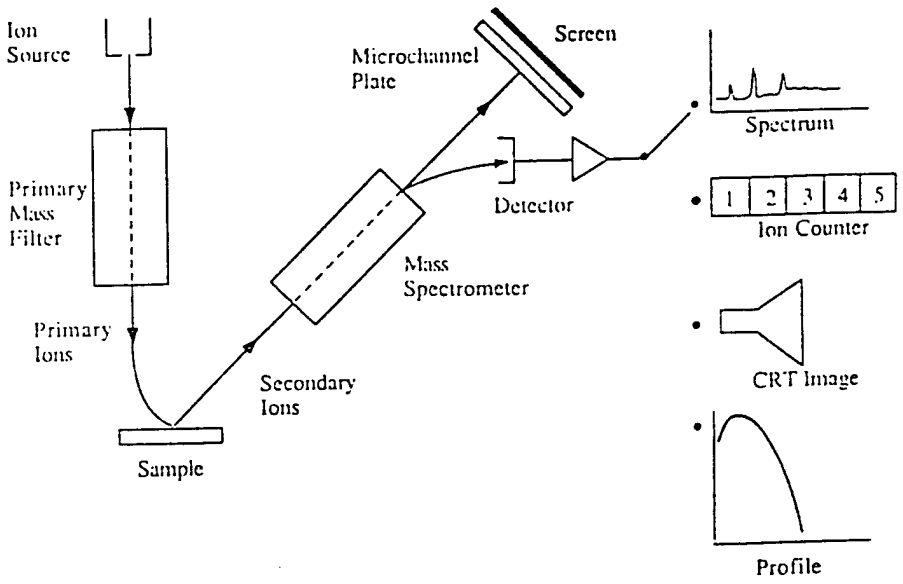

Fig. 2.6 SIMS Schematic.

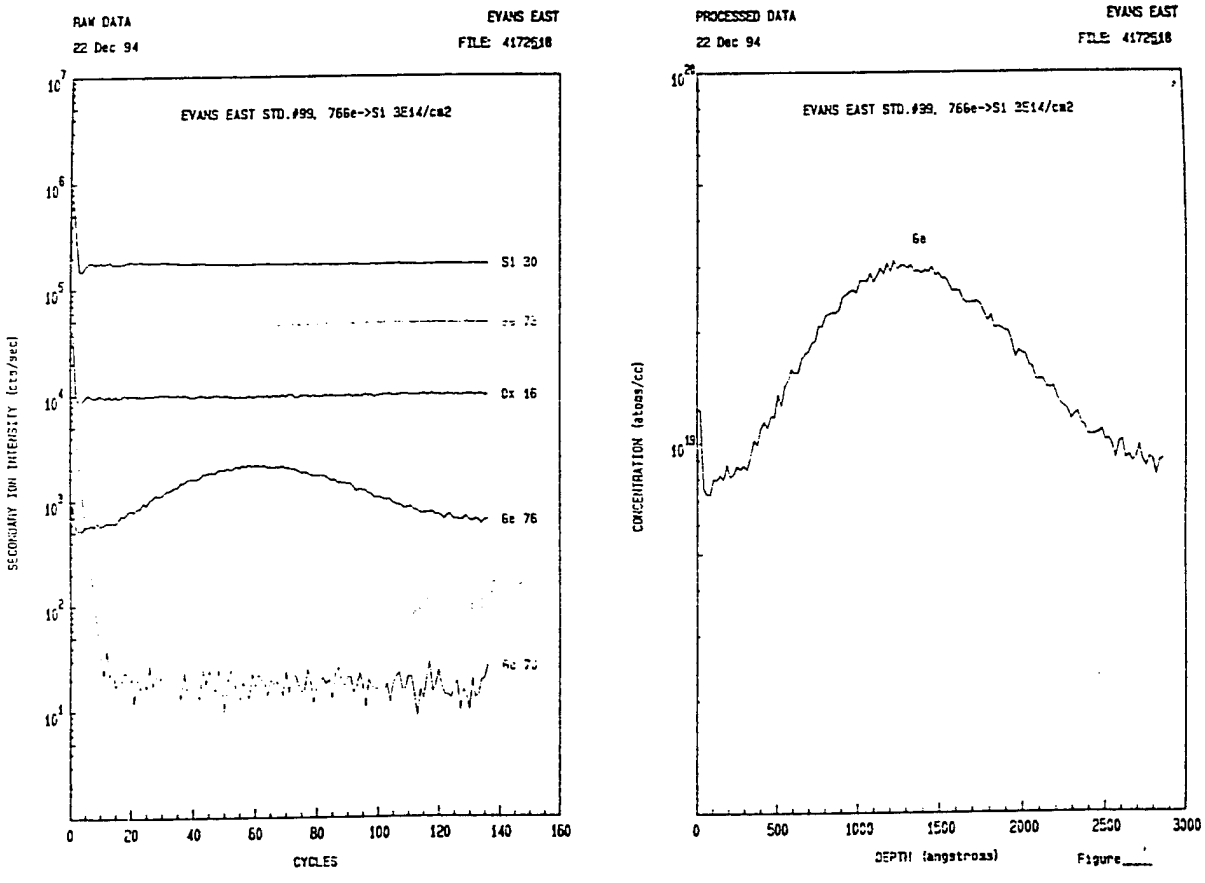

Figure 2.7 Raw and processed SIMS data. The plots on the left are secondary ion intensity signals in cts/sec versus time cycles. The plot on the right is processed profile of ^{76}Ge concentration versus depth.

Chapter 3: Results and Discussion

3.1. Introduction

The experimental work concentrated on continuation of the work done at Sherman Fairchild Laboratory of Lehigh University by Ta-Cheng Lin.[2] Lin investigated the effects of Ge implantation on the electrical characteristics of MOS devices. He showed that the population of hot carriers in Si was strongly reduced by the Ge implantation. However, for higher Ge implantation doses than $10^{14}/cm^2$ he observed a significant increase in the density of interface traps, and so he established the Ge implantation dose of $10^{14}/cm^2$ as optimal. Further he studied the effect of implantation peak location on the hot carrier injection, and determined the optimum peak location to be at the Si/SiO_2 interface.

Lin's next observation was a dramatic increase in the trapping rate in the oxide in the Ge implanted samples. This rate increased with the Ge dose. To eliminate this negative effect, he proposed a method of implanting a sample before oxidation. However, with this method, even though the charge trapping was significantly reduced, only a very weak reduction of the hot electron effect was achieved.

In my research I attempted to compromise between the method proposed by Lin, and investigate the cases when some of the oxidation was performed before the Ge implantation, and some after. Four cases were studied and compared:

1. Ge implanted at the Si/SiO_2 interface, no additional oxidation. Marked 'None'.

2. Ge implanted at the Si/SiO_2 interface, 3 minutes additional oxidation. Marked '3 min'.

3. Ge implanted at the Si/SiO_2 interface, 30 minutes additional oxidation. Marked '30 min'.

4. Control sample, no Ge implanted. Marked 'Control'.

These cases were studied and whenever possible, the results were compared and/or matched with Lin's.

3.2. C-V Characterization

High frequency CV curves were obtained for each of the samples. The results are plotted on Figure 3.1. From the graph it is apparent, that the curves get stretched out with additional oxidation time. This suggests that the interface trap density increases with additional oxidation time. This observation is in accordance with Lin's observation of a larger stretch-out and increase of the strong inversion capacitance for the case of oxidation after implantation.

3.3. Avalanche Injection Measurements

3.3.1. Hot Electron Effect Reduction

The results of the avalanche injection current versus gate voltage amplitude measurement are shown on Figure 3.2. Ge implantation has proven a strong means to reduce the hot electron effect in a MOS device. Additional oxidation does not seem to reduce the hot electron effect as we expected; on the contrary, it appears to be

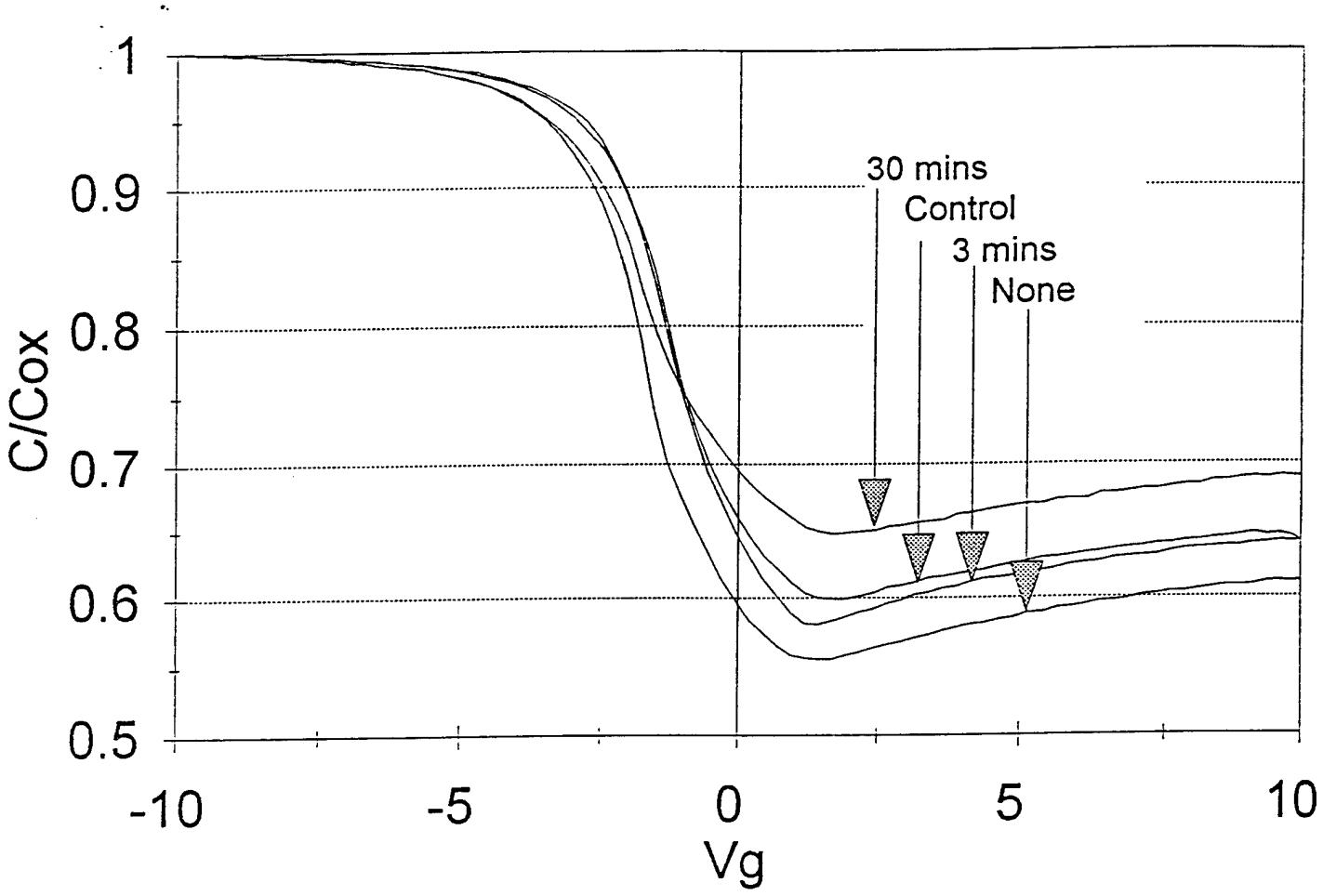

Figure 3.1 The CV curves for the four studied cases.

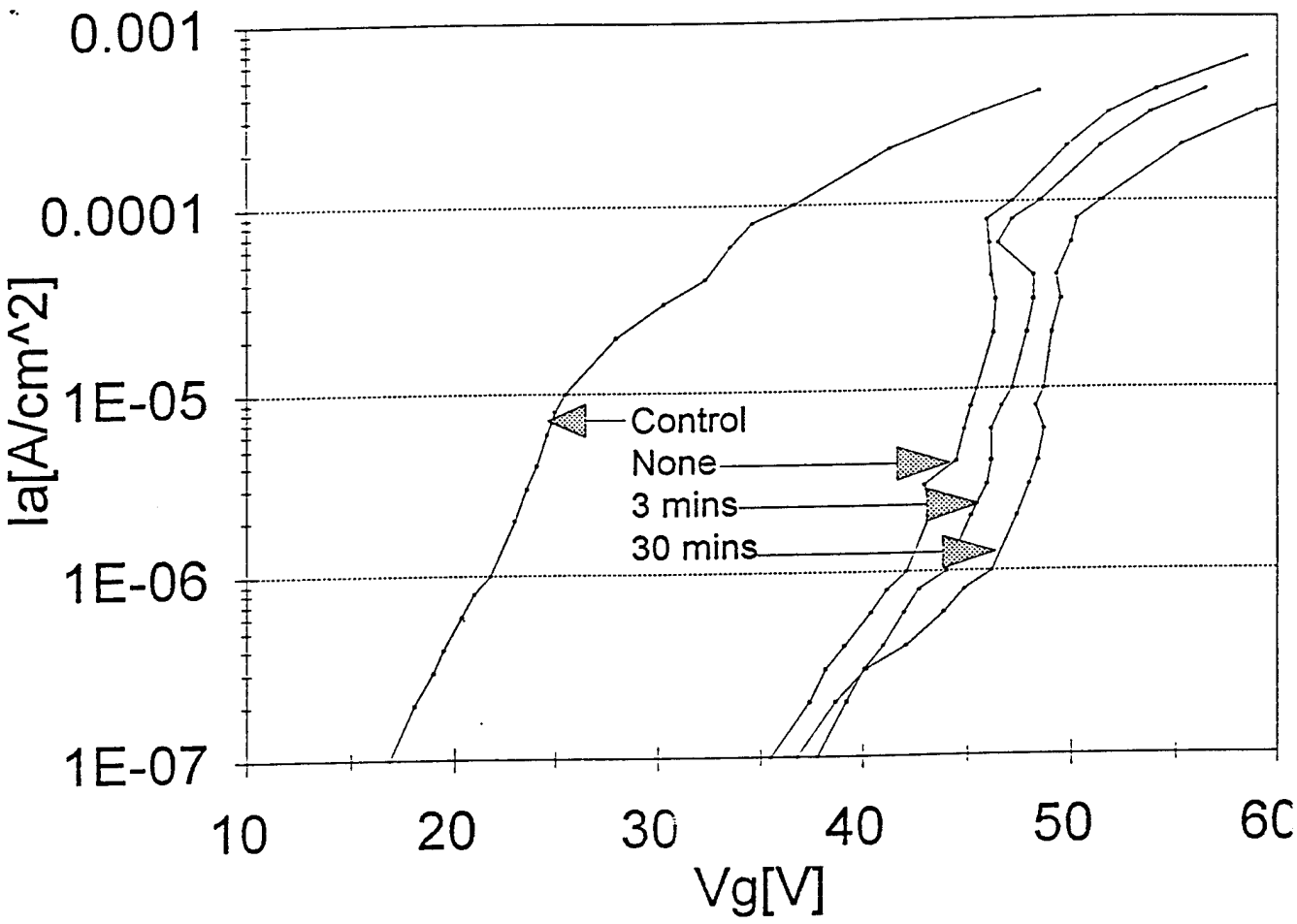

Figure 3.2 Avalanche current versus gate voltage signal amplitude curves for the four studied cases. These curves indicate the hot electron effect reduction.

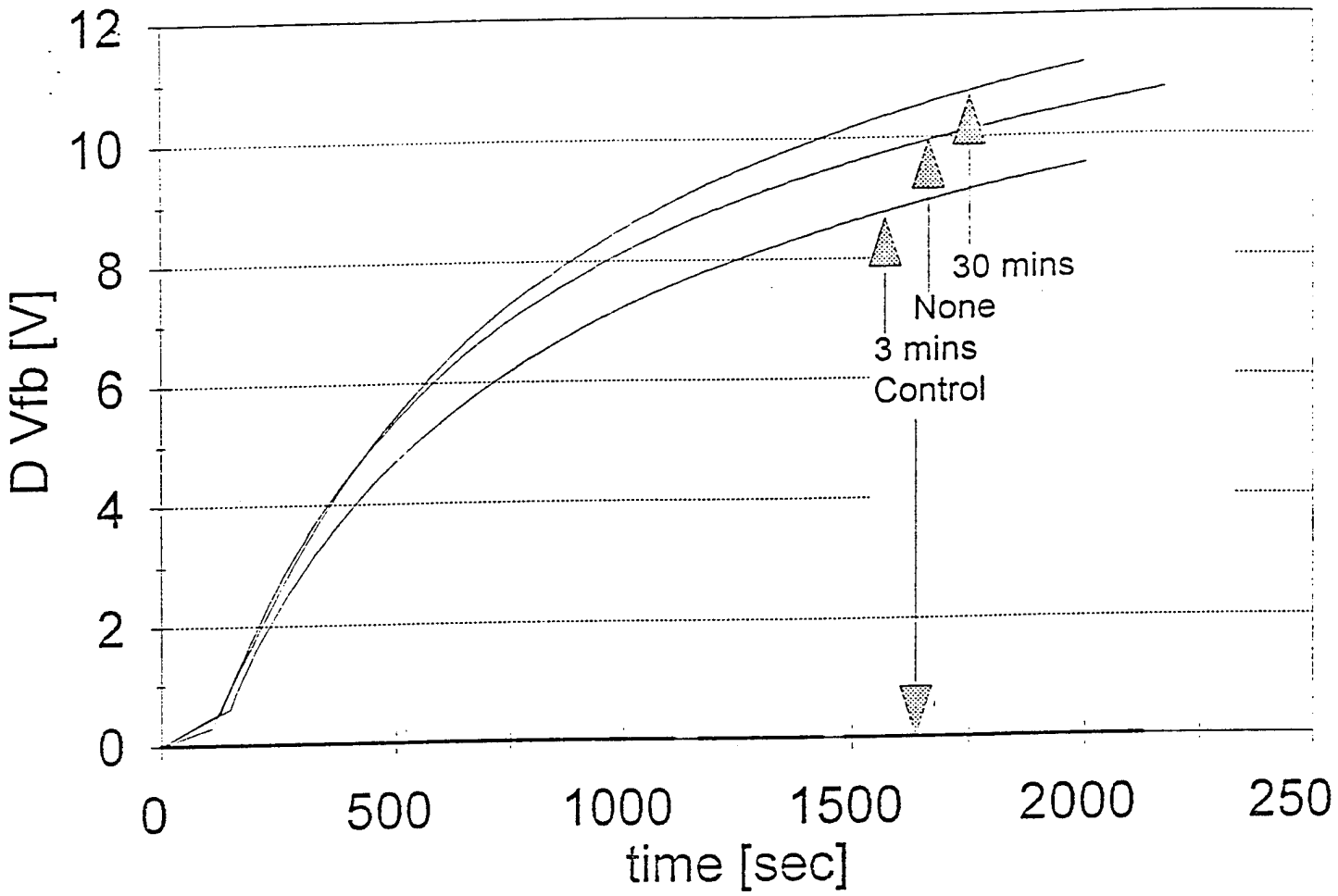

Figure 3.3 Flatband voltage shift versus time curves for an avalanche current density of 10^{-7} A/cm^2 indicate electron trapping rate in the oxide.

slightly enhancing it. This result comes also unexpected compared to Lin's observation of almost no hot electron effect reduction if the sample was oxidized after implantation.

3.3.2. Charge Trapping Study

The results of the charge trapping measurement performed for the avalanche current density of 10^{-7} A/cm^2 are shown in Figure 3.3. The control sample shows basically no tendency towards a flatband voltage shift in the duration of the measurement which was approximately 2000 seconds. Even though Lin's sample oxidized after Ge implantation followed the control sample very closely, when the oxidation was performed in part before and in part after oxidation, no noticeable reduction in oxide charge trap density was observed. The differences between the curves of Ge implanted samples on Figure 3.3 are within the range of accuracy of the method.

3.4. Secondary Ion Mass Spectroscopy (SIMS).

The SIMS plots in Figures 3.4 through 3.8 show germanium profiles for various combinations of pre and post Ge implantation oxidations. Here are brief explanations to each of the figures.

Figure 3.4 is a sample made for SIMS calibration. The sample was oxidized to 540 Angstroms and had ^{70}Ge implanted so that the peak of the implantation occurs in the middle of the oxide layer, that is approximately 270 Angstroms. The sample was annealed in N_2 for 30 minutes at 1000 °C. The resulting profile shows the original implantation

peak in the middle of the oxide layer, and some germanium buildup at the Si/SiO_2 interface.

Figure 3.5 is basically the same sample as Lin's oxidation after implantation. The germanium was implanted into silicon so that the position of the peak is exactly where the Si/SiO_2 interface would be after the sample is oxidized. The plot shows that germanium was strongly rejected from the oxide during oxidation and it piled up on the Si/SiO_2 interface.

The figures 3.6, 3.7, and 3.8 represent the pre and post Ge implantation oxidation cases of our study. From these figures it is obvious that germanium has a very strong tendency to migrate from SiO_2 to Si, especially in the region of the interface. Even though the initial germanium implanted in the oxide up to about midpoint of the original oxide remains the same for every case regardless of additional oxidation, the region where the oxide grew after implantation is strongly depleted of germanium. This is especially apparent in Figure 3.8. The peak Ge concentrations of the three cases are also slightly higher for the longer additional oxidation times: While in the case of no additional oxidation the peak is approximately at 3.8×10^{20} cm^{-3}, after 3 minutes of additional oxidation it increased to about 4.3×10^{20} cm^{-3}, and after 30 minutes to 5.5×10^{20} cm^{-3}.

3.5. QV Method To Determine The Density Of Interface Traps

Figure 3.9 presents the interface trap densities for the four cases under study. There is an apparent trend of increasing D_{it} with Ge implantation, and with the additional oxidation time.

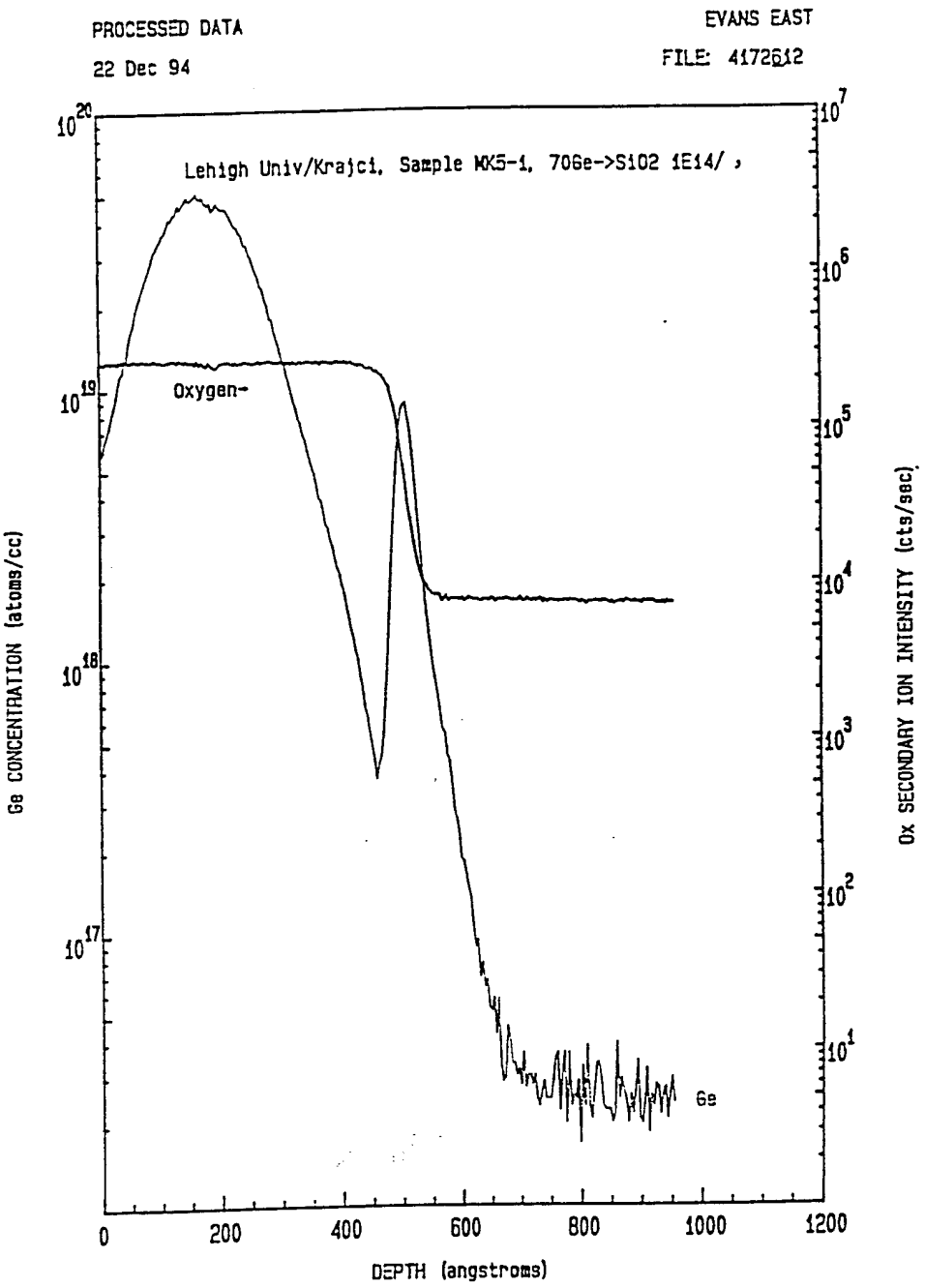

Figure 3.4 Germanium doping SIMS calibration profile. Germanium was implanted so that the peak occurs in the middle of the oxide layer.

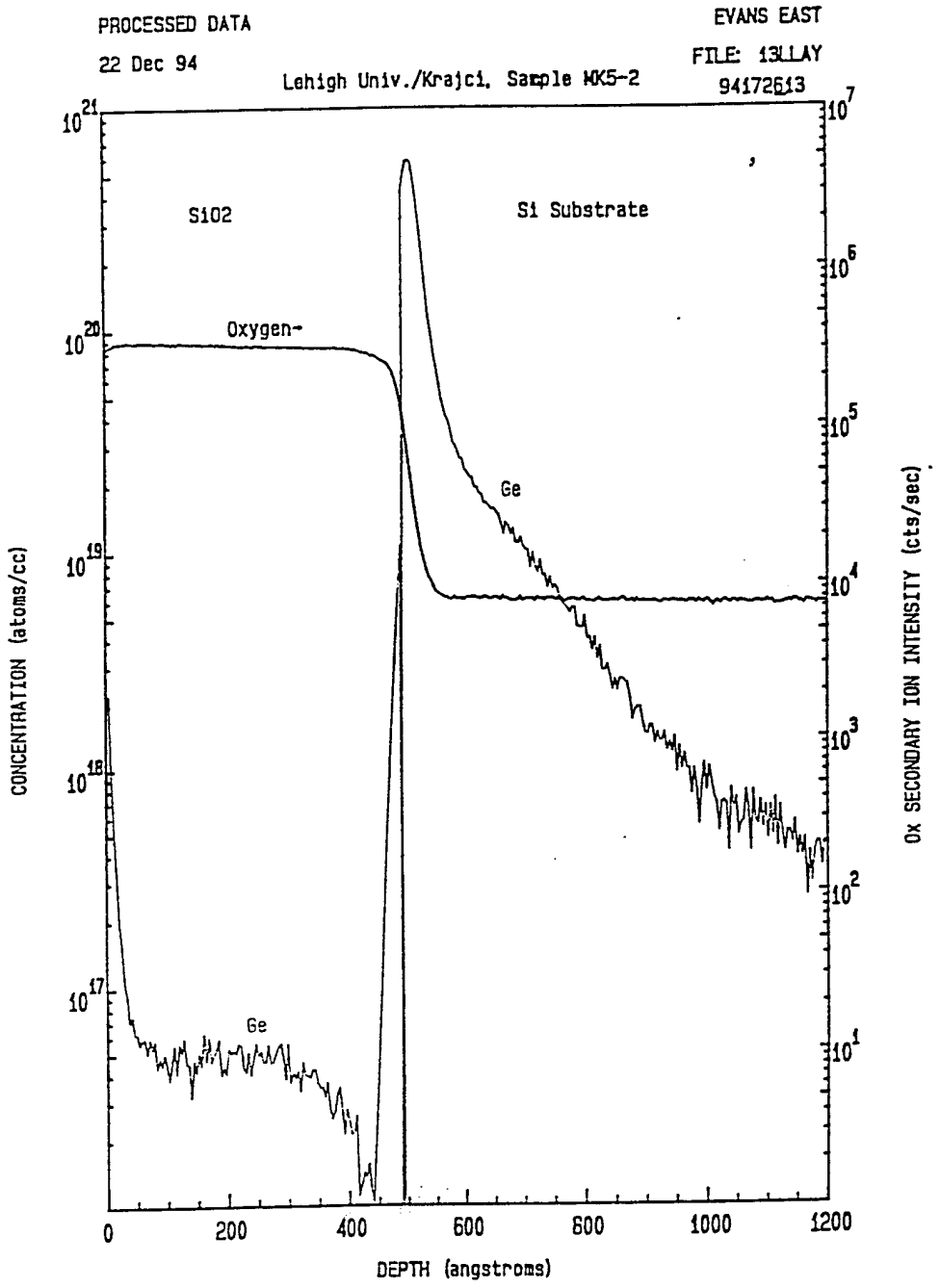

Figure 3.5 SIMS germanium profile for the case when germanium was implanted before oxidation.

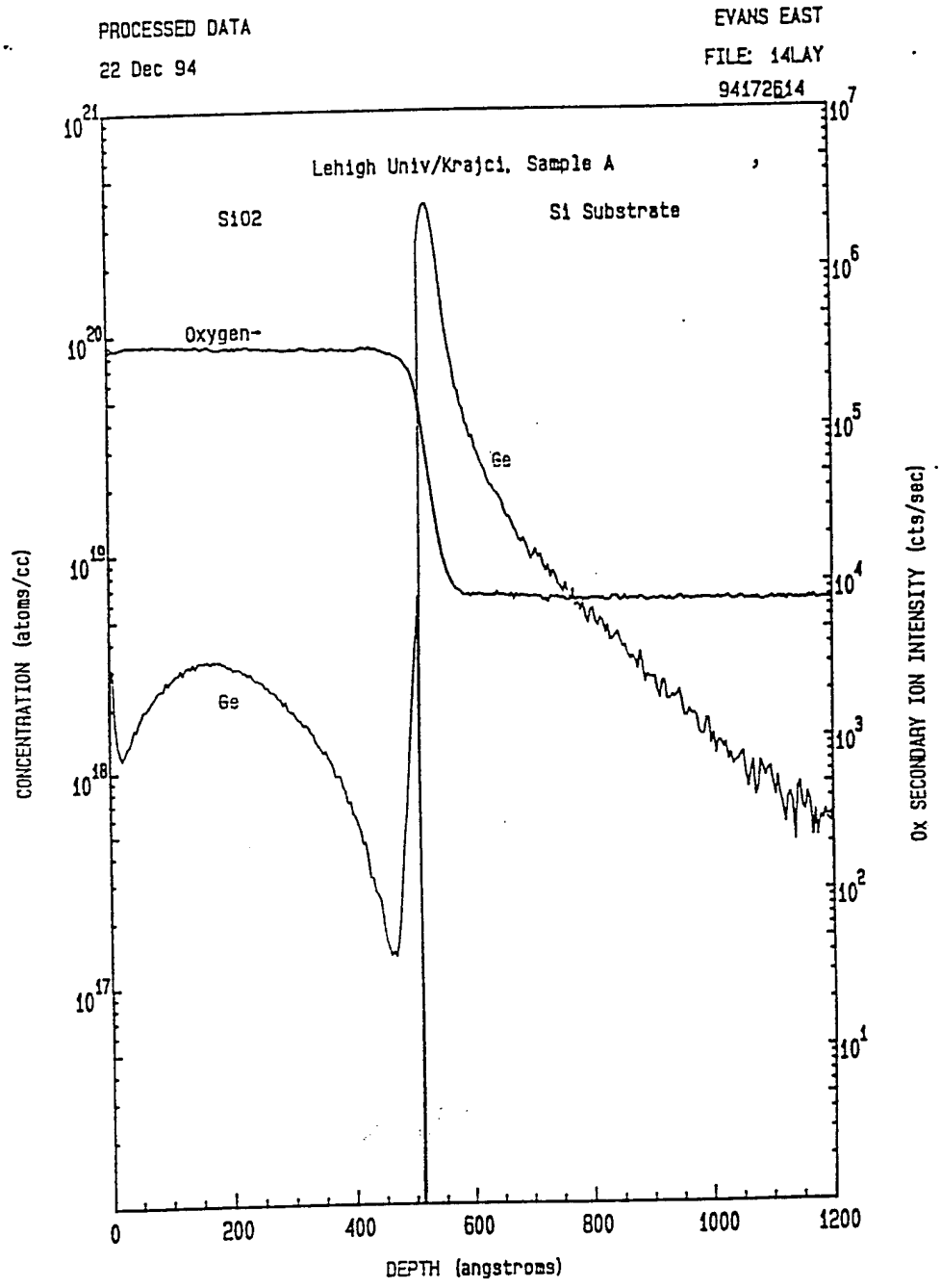

Figure 3.6 SIMS germanium profile for the case when germanium was implanted at the Si/SiO_2 interface. No additional oxidation was performed.

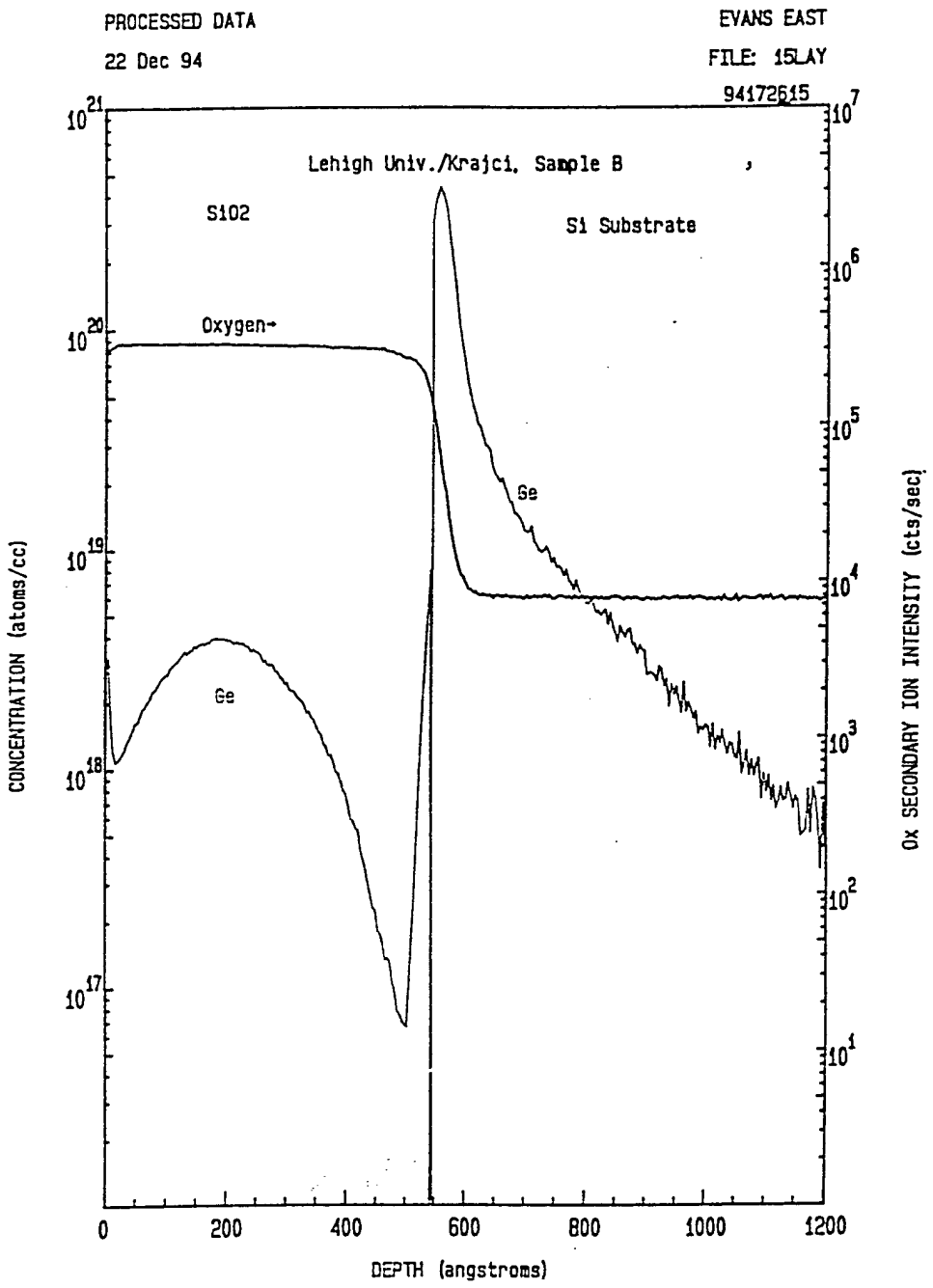

Figure 3.6 SIMS germanium profile for the case when germanium was implanted at the Si/SiO_2 interface. 3 minutes additional oxidation was performed.

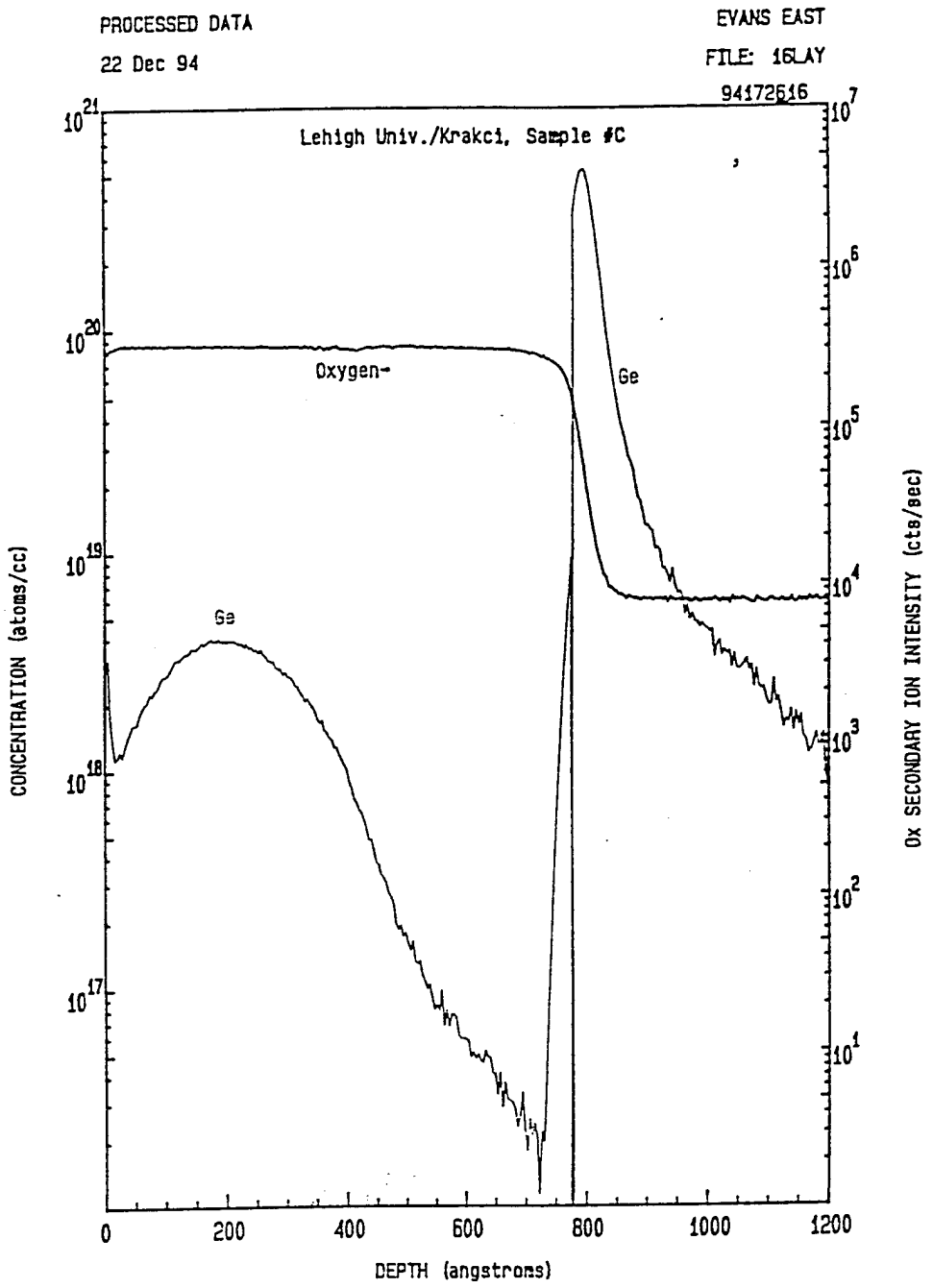

Figure 3.8 SIMS germanium profile for the case when germanium was implanted at the Si/SiO_2 interface. 30 minutes additional oxidation was performed.

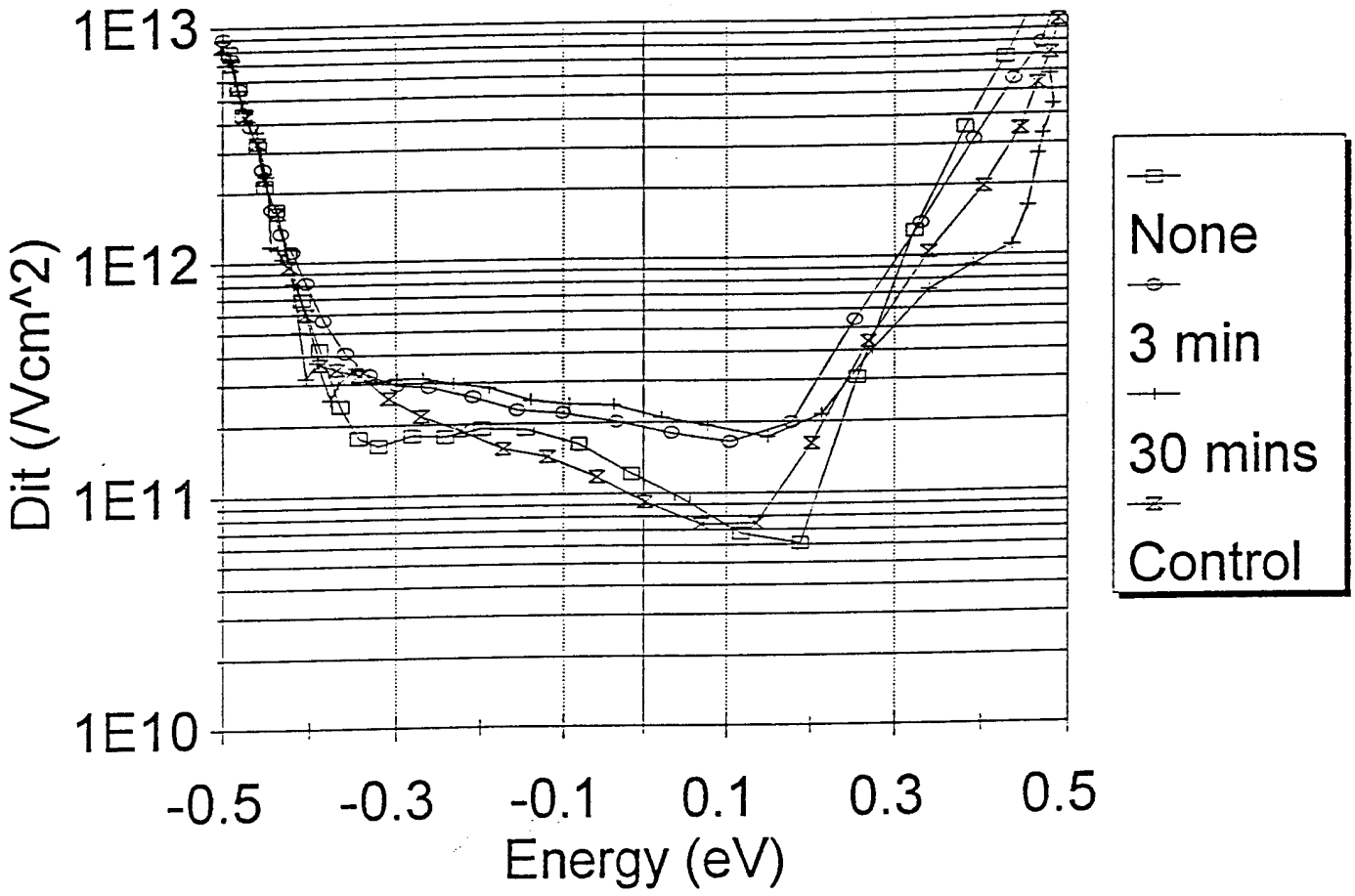

Figure 3.9 Interface trap densities for the four studied cases as determined by the QV method.

Chapter 4: Summary and Conclusions

4.1. Summary

This research study has helped us gain some insight into the process of silicon oxidation when germanium is present, and into further approaches towards utilizing the method of germanium implantation for reduction of the hot electron effect for small MOS devices used in very large scale integration (VLSI).

4.2. Analysis

Based on the presented results, we can form the following hypothesis of what is happening with germanium during the process of oxidation, and how it affects the electrical characteristics of a MOS device.

Even though germanium shows a very strong tendency to be rejected from the SiO_2 and pile up in Si near the interface, some of it remains present in the oxide. A surprising result came up by comparing Lin's case of oxidation after Ge implantation with the case of 30 minutes additional oxidation after the implantation. Even though both cases show very similar profiles of Ge distribution around the Si/SiO_2 interface as determined by SIMS, the reduction of the hot electron effect was very different: while the hot electron effect is significantly reduced when germanium was implanted into some SiO_2, this reduction is minimal when the implantation is into plain silicon. Lin expressed hypothesis that the optimal location of Ge implantation peak for maximum hot electron effect reduction is at the Si/SiO_2 interface. However, he only studied cases when the Ge implantation peak was in the silicon, not in the oxide. Therefore it is also possible that the

hot electron effect could be further reduced if the peak of the Ge implantation were placed in the oxide, and thus more germanium would be present in the oxide bulk. *It seems that it is the presence of germanium in the bulk oxide that is directly related to the reduction of the hot electron effect.* It remains a subject of further studies to examine the mechanism of this relationship actually is. It is possible that germanium in the oxide is incorporated in a partially oxidized state as GeO and the bonds that do not form into the network are involved in this observation.

This study also fully supports Lin's hypotheses that the presence of Ge in the bulk oxide is responsible for the increases in the trapping rate, and that piling up of germanium on the silicon side of the Si/SiO_2 interface increases the interface trap density.

4.3. Suggestions for Future Studies

Since it has become obvious that it is the germanium piled up on the silicon side of the Si/SiO_2 interface which increases the interface trap density, and that any thermal treatment causes migration of Ge atoms near the interface from SiO_2 to Si where it piles up, a process should be designed which minimizes the chances of germanium piling up near the interface in silicon. Should my hypothesis of the hot electron effect reduction being directly related to the presence of germanium in the bulk oxide prove correct, it would leave only two variables in the game: hot electron effect reduction on one side, and increased trapping rate on the other, and it would be only a matter of finding the optimal amount of germanium placed in the oxide to give a solution to the problem of hot electrons without negatively affecting other important parameters.

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Appendix:Fabrication Sequence for MOS Capacitors

1. **Staring Material:**

   3 inch Si wafer, p-type, Bdoped, <100>, .14-.17 ohm-cm

2. **Oxidation**

   RCA clean

   oxidation: 1000°C, 45 minutes, dry oxide, ~500Å

   anneal: 1000°C, 15 minutes, 1.5 l/min N_2

3. **Ge Implantation**

   implantation: Ge, 73 keV, 10^{14} cm^{-2}

   additional oxidation 3, 30 minutes, 1000°C, dry oxide

   anneal: 700°C, 15 min, 1.5 l/min N_2

4. **Metallization**

   Al deposition: evaporator

   photo: define gate area, 1mm×1mm

   etch: Al, PAN etch, 45°C, 3 minutes

   strip PR: PRS-2000

   anneal: PMA, 450°C, forming gas (H_2/N_2, 1:5)

Note: Indent indiactes steps performed only on selected wafers.

Vita

Martin Krajci was born on January 12, 1970, in Bardejov, Slovakia (formerly Czechoslovakia) to Mr. Albin Krajci and Mrs. Klara Krajciova.

In 1988 he started attending the University of Transport and Communications in Zilina, Slovakia, majoring in electrical engineering. In 1990 he was selected a scholarship recipient under the Freedom Lamp program, a project of the new democratic Slovak government with several US universities, and was assigned to study at Wilkes University in Wilkes-Barre, PA. He graduated from Wilkes University in 1993 summa cum laude with Bachelor of Science in electrical engineering. In August 1993 he started his graduate study at Lehigh University Department of Electrical Engineering and computer science as a research assistant in the group of Prof. R. Jaccodine. In June 1995 he took a position of electronics engineer in Artann Laboratories, East Brunswick, NJ.

CHARACTERIZATION OF GERMANIUM IMPLANTED MOS DEVICES

by
Ta-Cheng Lin

A Dissertation
Presented to the Graduate Committee
of Lehigh University
in Candidacy for the Degree of
Doctor of Philosophy

in

Electrical Engineering
Lehigh University
1994

Certificate of Approval

This dissertation is approved and recommended for acceptance in partial fulfillment of the requirements for degree of Doctor of Philosophy.

(date)

Professor in charge

Accepted:

(date)

Special Committee directing the
doctoral work of
Ta-Cheng Lin

Chairman

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Finally, I would like to thank my parents, parents in law, brother and sister for their love and support. Most importantly, my wife Liang-Yi E. Cheng, to whom this dissertation is dedicated, who assisted in preparing the manuscript and shares my bitterness and happiness. The work reported in this dissertation was supported by grant from the Army Research Office and the Office of Naval Research.

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Abstract

To meet the higher demands of the functional capability in modern digital circuitry, MOS transistor dimensions have been decreased dramatically with a comparable decrease in the channel length. With the reduction in channel length, short channel effects became the first concern in designing these devices. Scaling theory shows that short channel effects can be avoided by reducing the dimensions and operating voltage by a factor K while increasing the substrate doping density by the same factor. However, with the increase of the doping density in the channel and the non-scalability of the operating voltage, very high electric fields are produced within the device. A large number of the carriers can be accelerated by the high electric field to energy high enough to surmount the energy barrier between the silicon and insulator. This phenomena is called the hot carrier effect which is a serious problem in today's deep submirometer MOSFET's. For example, the hot carriers in the MOSFET can cause degradation in performance due to interface states build-up at the drain which reduces the transconductance and a shift in threshold voltage when they are trapped in the insulator. A lot of work has been devoted to the modeling of hot carrier injection and the physical mechanisms of hot carrier induced degradation, less work has been done to reduce the hot carriers injection. The well known method is to us a lightly-doped-drain (LDD) structure. However, as the device dimension shrinks below 0.5 μm, the LDD structure begin to decrease the current gain. The search for an alternative method to reduce the hot carrier effect has become an urgent problem.

Ge implantation has recently been found to reduce hot carrier effects. This technique shows promise but has not yet been optimized. This dissertation aims at the investigation of the effect of Ge implantation on the electrical properties of MOS devices. The avalanche injection technique was used to study the hot carrier energy distribution in the silicon. To study the Si-SiO_2 interface, we have developed an accurate and direct method using an improved Q-V technique to evaluate the interface state densities. The charge trapping property of the Ge implanted SiO_2 has also been studied. By varying the implantation dose and energy, we determine the optimum implantation condition for the Ge implantation technique. The optimum dose is 10^{13} /cm^2, energy is 70 KeV. The effect of Ge implantation on the n-channel MOSFET mobility has also been investigated by measuring the I-V curves of operating devices.

Chapter 1
Introduction

1.1 Background

Since the discovery of transistor in December 1947 by Bardeen and Brattain, the semiconductor revolution can be divided into three periods[1]: The first period began with the invention of transistor. The important inventions in this period included the bipolar junction transistor, the demonstration of the silicon MOS transistor and the integrated circuits. The second period which is known as the era of SSI (Small Scale Integration) and MSI (Medium Scale Integration) took off when the integrated circuit was first invented in 1958[2]. The achievements in this period include many processing breakthroughs and characterization techniques that overcome earlier difficulties in device fabrication. For example, the understanding of Si-SiO_2 system[3,4,5], the inventions of LOCOS[6] (Local Oxidation) technique and polysilicon gate structure[7] etc.. The third period began with the invention of the 1-Transistor DRAM (Dynamic Random Access Memory) cell[8] and the 6-Transistor SRAM cell and we are now two decades into this period. The major achievement in this period is the scaling down of the device geometry. In the early 1960's the feature size of the transistor was greater than 10 μm, today the feature size of transistor has been reduced to sub-micrometer. Our semiconductor technology has advanced from small scale integration (SSI) to large scale integration (LSI) and recently to the very large scale integration (VLSI). The steady progression toward smaller and smaller devices can be seen in figure 1.1 which shows the feature

size of DRAM MOS memory and component count per chip.

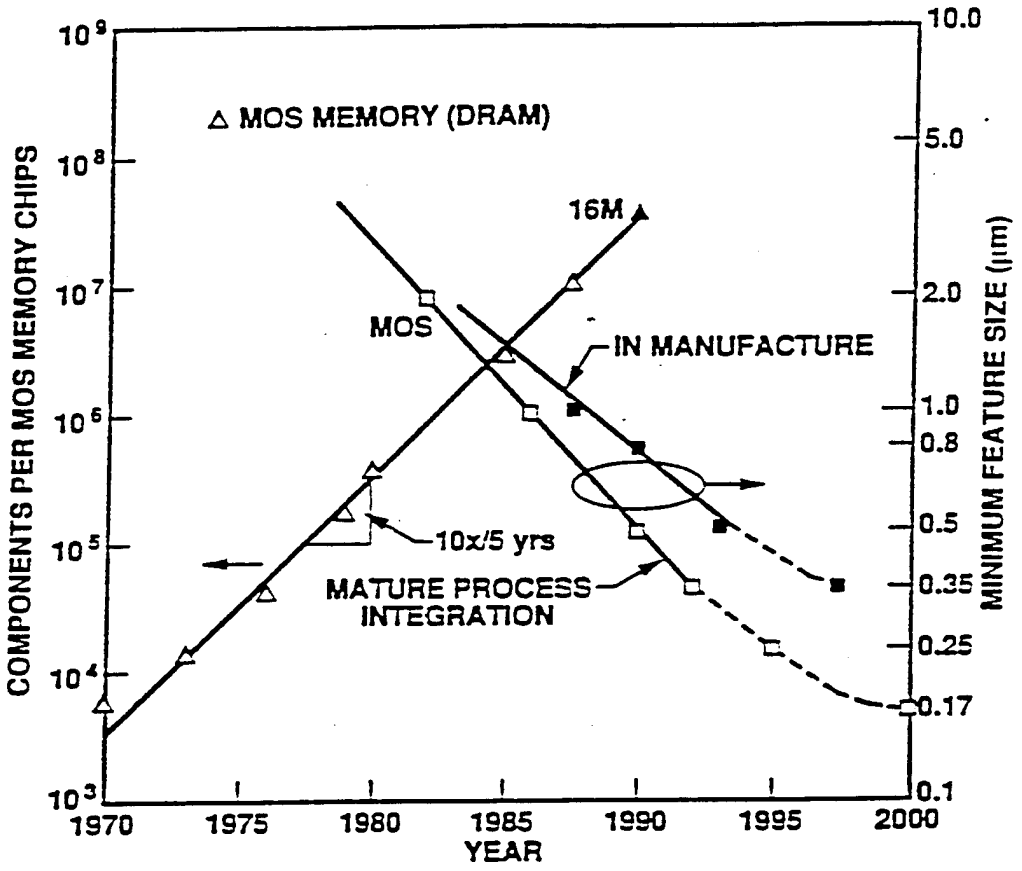


Figure 1.1 MOS memory component growth and feature size reduction vs calendar year.

The reasons for the trend toward smaller devices size include:

(1) The delay times associated with the charging of gate capacitances, and parasitic capacitances are reduced, so the circuit speed is increased.,

(2) As device dimensions have decreased, integrated circuits have included many more component transistors, and the cost per functional block has been reduced. and

(3) Fewer packages and boards are necessary to implement a circuit function, so the system reliability is enhanced.

We expect this trend will continue in the future. However, with the reduction in channel length of MOSFET, device-related problems and limitations to further size reduction have appeared. In the following sections, we will review the effects related to the scaling down of devices discovered by former researchers.

1.2 Geometric Effects

1.2.1 Threshold Voltage Modification

In long channel MOSFET's, the gradual channel approximation[9,10] is used to predict the threshold voltage. This approximation states that the gradient of the field in the direction of current flow is much smaller than the gradient of the field in the direction perpendicular to the silicon surface, so the threshold voltage is only a function of gate voltage.

In 1973, H.S. Lee[11] found the threshold voltage of the short channel device not only depends on gate voltage, but on channel length and drain voltage. Figure 1.2 shows

the threshold voltages in short channel devices.

This phenomenon can be explained as follows: In short channel devices, the channel length becomes comparable to the junction depth and the depth of the depletion region. The potential distribution in the channel now depends on both the transverse field and the longitudinal field. In other words, the potential distribution becomes two dimensional, so the one dimensional gradual channel approximation is no longer valid.

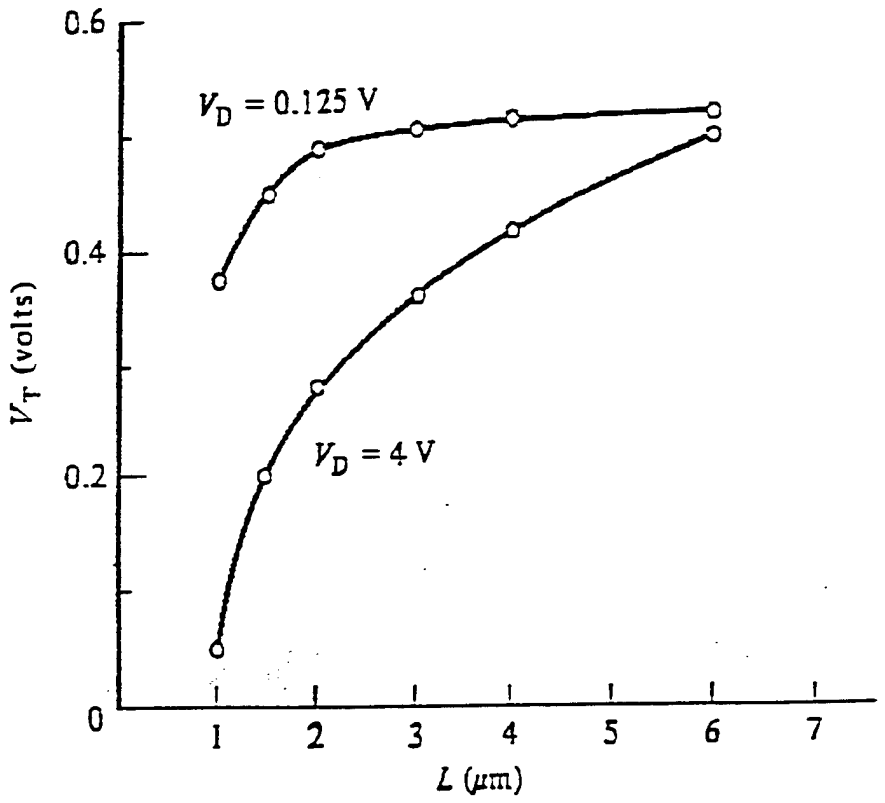


Fig. 1.2 Observed threshold-voltage variation with channel length and applied drain bias in short-channel MOSFET's[77].

1.2.2 Punch Through

Another geometric effect in short channel device is the punch-through effect. When the source and drain are separated by a few microns or less it becomes possible for the p-n junction depletion regions around the source and drain to touch or punch-through[12] as pictured in fig. 1.3.

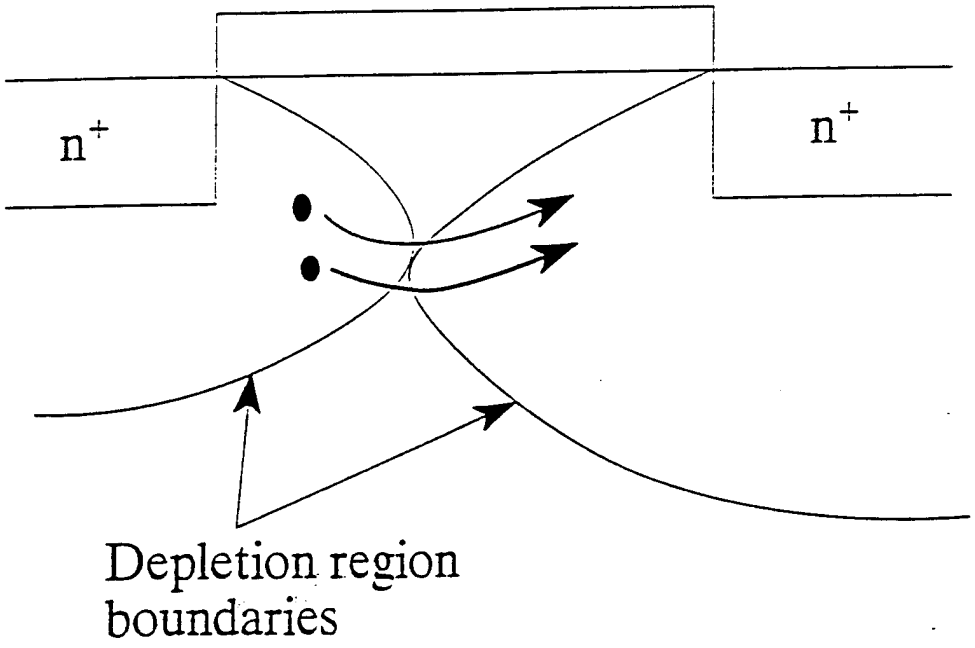


Figure 1.3 Punch-through and space-charge current in a short-channel MOSFET

When punch-through occurs, a significant change takes place in the operation of MOSFET, the gate loses control of the current. The source to drain current is then no longer constrained to the surface channel, but begins to flow beneath the surface through the touching depletion regions.

The geometric effects discussed above occurred because only the surface dimensions are reduced while other circuit and device parameters remain unchanged. To solve this problem, Dennard et al[13] proposed the constant electric field scaling theory. This theory states that geometric effects can be avoided by reducing the device dimension and operating voltage by a factor K while increasing the substrate doping by the same factor. The parameters of the scaling theory are listed in table 1.1.

Note, the voltage and current are scaled by a factor 1/K. This was applicable in the early 1970's when supply voltages were reduced from 16V, to 12V, to 8V and finally 5V. In recent integrated circuit applications, however, there is a reluctance to scale down the operating voltage as the original scaling law dictates, since this will reduce noise margin and circuit speed. Since the applied voltage is not scaled down and the doping density is scaled up, there is a higher electric field inside the MOSFET device. This high electric field is the source of hot carriers which induce the most serious degradation problem in today's ultra small devices.

Parameters	Scale(K > 1)
L, W, t_{ox}, X_j	1/K
Doping Concentration	K
Voltage	1/K
Current	1/K
Delay Time	1/K
Capacitance	1/K
Power Dissipation	$1/K^2$
Power Delay Product	$1/K^2$
Power Density	1

Table 1.1 Conventional Scaling Theory

Another quantity which fails to scale by the scaling theory is the slope of subthreshold transfer characteristics[14] which determines the leakage current in the normally off device. This can effect the off-state power dissipation, dynamic logic clock speed, and memory refresh time.

There are other problems that become more and more important in device scaling

such as contact resistance, source/drain diffusion resistance, and inversion layer capacitance[15]. The discussion of these problems can be found in reference 15.

1.3 High Electric Field Effects

The non-scalability of applied voltage combined with the shrinking of the device lateral dimensions has resulted in a number of effects on device characteristics that are caused by the high electric field. This high field can cause serious problems in the device. First, the velocity of the carriers will saturate. Secondly, the carriers will obtain very high energy from the field and can be injected from the silicon into the SiO_2 insulator. The phenomena induced by high electric fields and their effects on the device will be presented next.

1.3.1 Velocity Saturation

In long n-channel MOSFET's, the field is lower than 20 KV/cm, the carriers lose energy through inelastic scattering (impurity and acoustic phonon scattering) and can remain in thermal equilibrium with lattice. Carrier transport is then ohmic and occurs in the conduction band. In this case, there is no theoretical limitation on velocity that carriers can attain in the surface channel. It is implicitly assumed the carrier velocities increase as needed to support the computed current. When the electric field exceeds approximately 20 KV/cm, optical phonon emission dominates the scattering process, and the electron's drift velocity saturates as illustrated in figure 1.4.

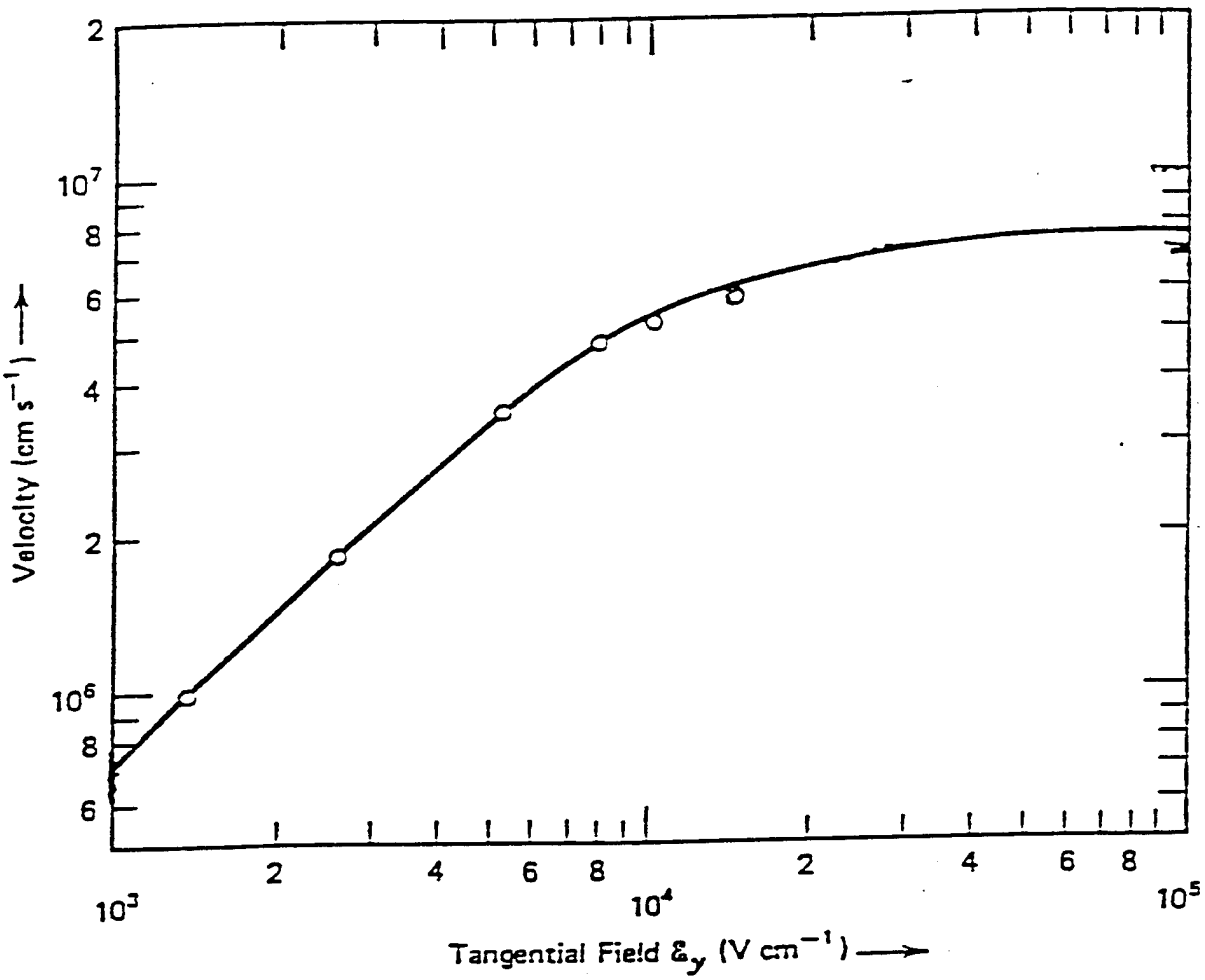


Figure 1.4 Velocity of electron in an MOS surface channel as a function of the tangential electric field[78].

Under this condition, current is no longer ohmic[16]. Velocity saturation has two main effects on observed characteristic as shown in figure 1.5. First, the current is significantly reduced. Second, the current at saturation exhibits an almost linear dependence on (V_G-V_T) as opposed to the conventional square law dependence.

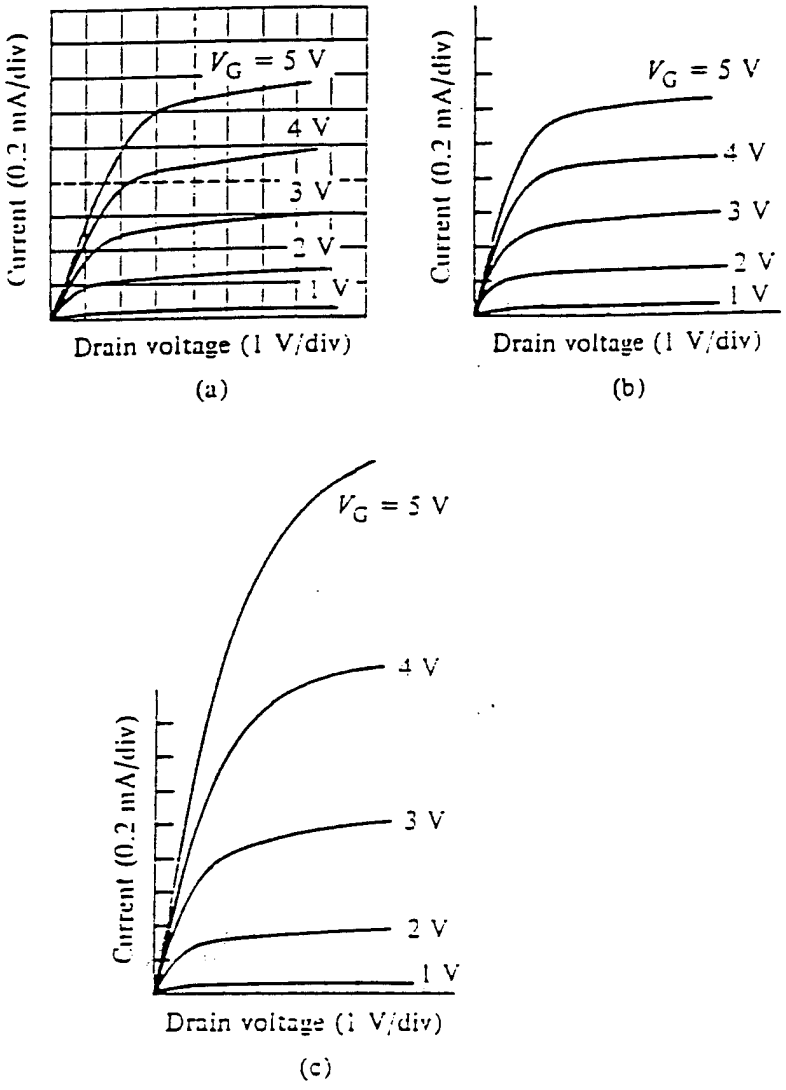


Fig. 1.5 Illustration of the effects of velocity saturation on the MOSFET I_D-V_D characteristics. (a) Experimental results derived a short channel MOSFET. Theoretical characteristics (b) including velocity saturation and (c) ignoring velocity saturation.[79]

1.3.2 Hot Carrier Effects

When the field strength reaches approximately 100 KV/cm, the electron gains more energy from the electric field between scattering events than it loses when it scatters. For fields exceeding this value, the electron is no longer in equilibrium with the lattice, and its energy relative to the conduction band edge begins to increase. The electron heated by this high field is called a hot electron. Under these conditions, two potential problems arise: First, electrons with energy greater than the threshold energy ϕ_I for impact ionization can create electron-hole pairs, the holes comprising the substrate current. Second, hot carriers impinging on the potential barrier at the Si-SiO_2 interface can be emitted into the oxide, leading to a generation of interface states as well as gate current. Some of these carrier can be trapped in the oxide and build up a negative charge. The sequence that leads to these two effects is shown in sequence of events in figure 1.6.

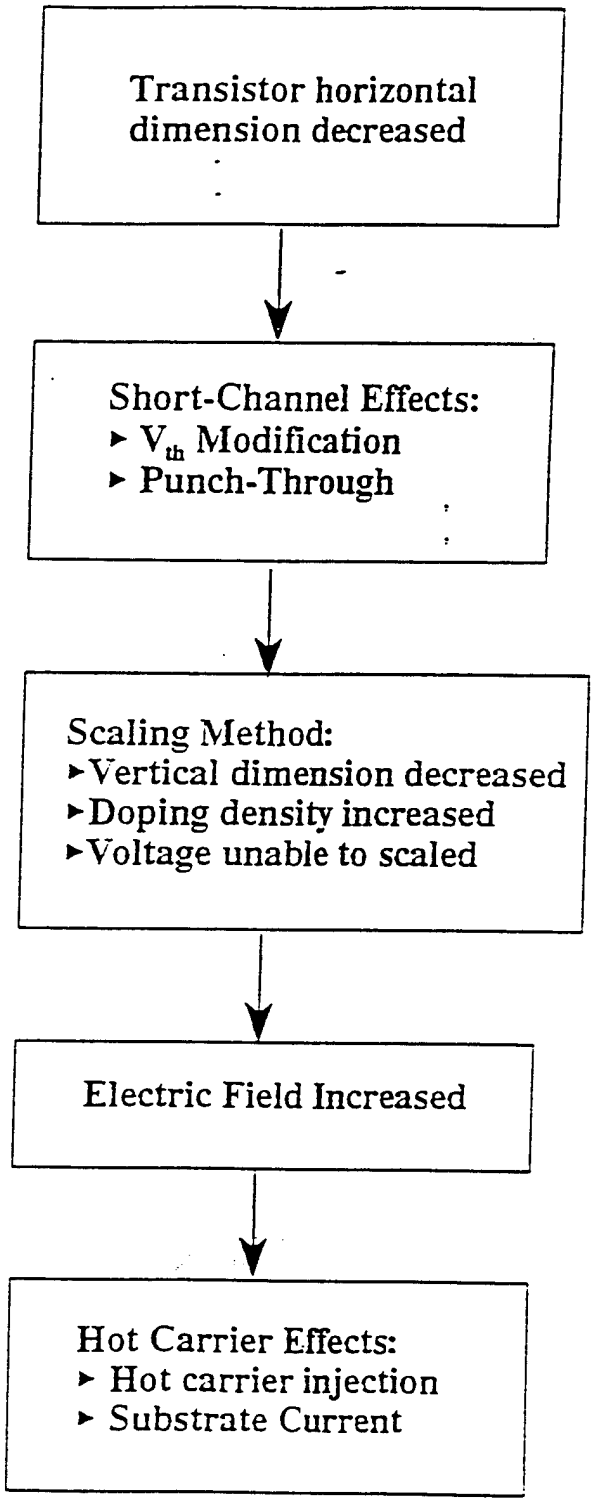


Figure 1.6 The sequence of events which has led to MOS device hot carrier effects.

1.3.2.1 Substrate Current

As shown in figure 1.7, impact ionization generates electron-hole pairs. The electrons accelerate toward the drain and holes flow to the substrate, appearing as substrate current.

Because of the high resistivity of the substrate material,

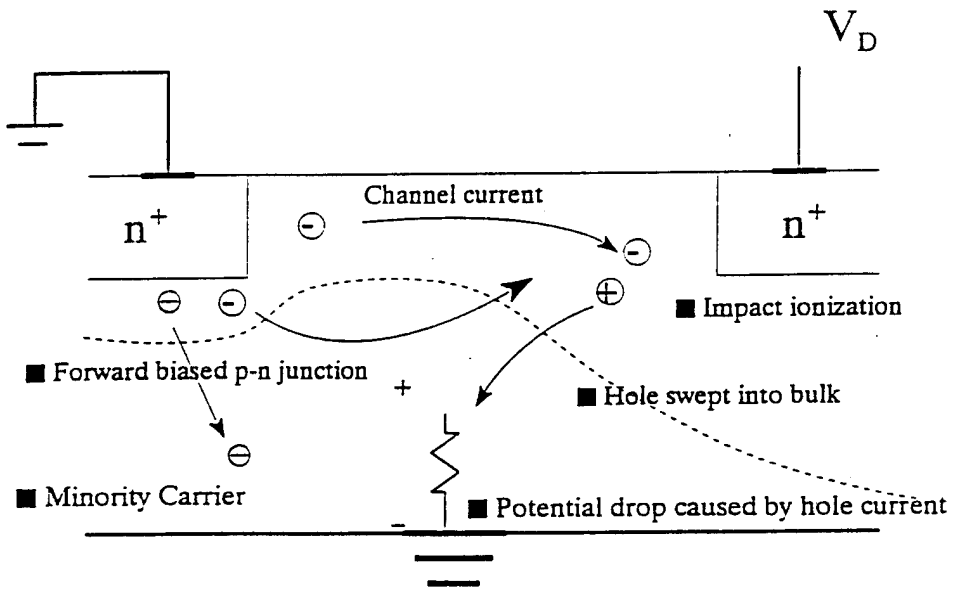


Figure 1.7 Visualization of substrate current generation and regenerative feedback, which can give rise to current enhancement in short-channel MOSFET's.

substrate current will cause a significant voltage drop across the substrate. If the substrate current is large enough, it will forward bias the source substrate junction and turn on the parasitic bipolar transistor. This can dramatically increase the drain current and cause MOSFET break down.

The latch-up[17] effect which can decrease the limiting power supply in CMOS structure caused by substrate current is a well-known problem in designing CMOS devices.

Some minority carriers can be generated by the forward biased source junction due to substrate current or Bremsstrahlung radiation[17,18]. The minority carrier has a long life time, so its existence could cause serious problem in devices.

In a dynamic RAM, the substrate minority carrier can degrade its holding time[19]. The minority carrier near the charge-coupled device (CCD), could add additional signal to the CCD output.

1.3.2.2 Hot Electron Emission

The high energy carrier "lucky" enough to travel to the Si-SiO_2 interface without suffering a scattering process can be injected into the gate insulator. Channel hot carrier injection into the gate has been recognized as a major cause for device performance degradation and instability due to electron trapping in gate oxide and/or interface state generation[20,21,22]. The emission current is widely studied as a monitor of degradation phenomenon and is a function of hot electron distribution in the silicon near the Si-SiO_2 interface. This hot electron distribution depends on applied voltages, the device parameters such as doping profile, junction depth, and the channel length and the ambient

temperature.[21]

Hu et al[73], were first to use the "lucky electron" concept to empirically explore the gate current. Their model can be described as follows: In order for the channel hot electrons to reach the gate, the hot electrons must gain sufficient kinetic energy from the channel field and with their momentum redirected toward the Si-SiO_2 interface in order to surmount the SiO_2 potential barrier. To quantify the probability that these electrons could eventually be collected by the gate, several types of scattering have to be considered. The scattering events are illustrated in Fig 1.8. From point A to B a channel electron gains energy from the channel field and becomes "hot". At B, re-direction of the hot electron takes place. From point B to C, the hot electron must not suffer any energy-robbing collision so that it will retain the energy required to surmount the Si-SiO_2 potential barrier. The hot electron must also suffer no collision in the oxide image potential well located between C and D. Once the hot electron arrives at location D, it will be swept toward the gate electrode by the oxide field. Later various modifications on the hot electron simulation methods have been proposed to tackle the deficiencies of the model. Kuhnet et al. improved the model to incorporate the nonlocal effect[74]. Ricò et al. have derived a numerical gate current model to further take into account the non-Maxwellian form of distribution function[75]. Chimoon Huang et al. proposed a method to approximate the high-energy tail distribution in the devices[76].

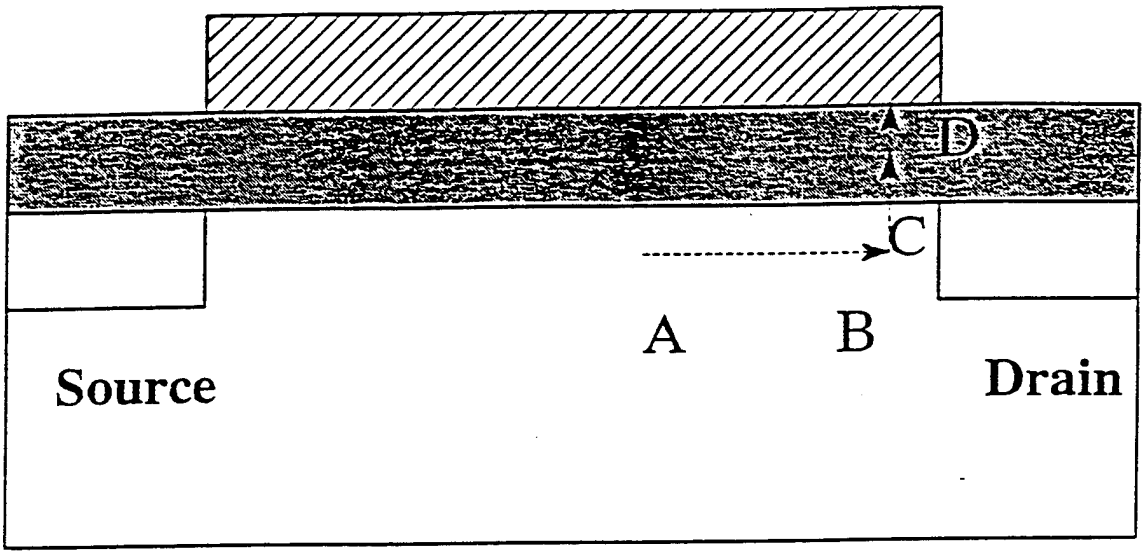


Figure 1.8 The three scattering probabilities in the 'lucky electron' model.

1.4 Hot-Carrier Degradation

Despite the large effort spent during the last few years to understand the physical origin of hot carrier induced degradation , no unanimous agreement exists on the mechanism involved. Initially, it was believed that oxide traps were primarily involved[25,26]. However, with the advent of the charge pumping technique[27], it is recently ascertained that interface state generation are solely responsible[28-33]. However, recent studies show that the type of damage depends on the stress condition.

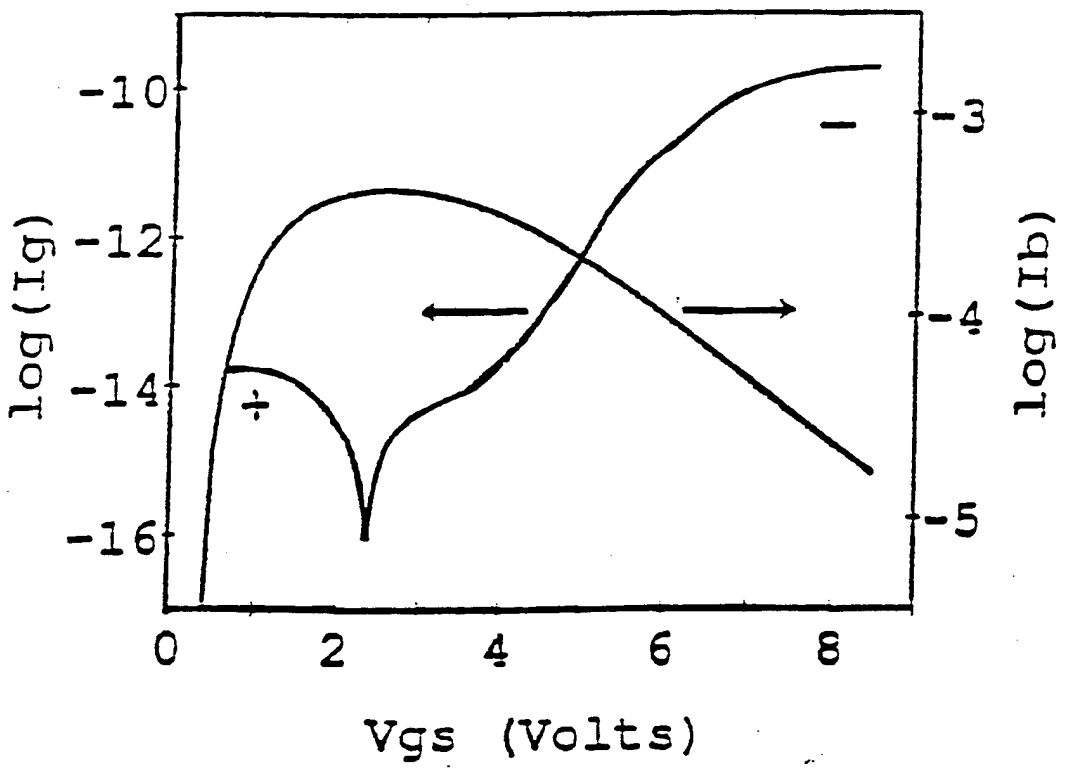


Fig. 1.9 Typical gate and substrate currents versus gate voltage obtain for n-MOS transistor.

1.4.1 Static Stress Hot Carrier Damage

The understanding of the types of damage has resulted from the study of the different components of the gate current arising during hot-carrier stress conditions. Figure 1.9 shows the gate current and substrate current as functions of gate voltage for a MOSFET at V_{DS}=7.0 V.

In the low gate voltage($V_{GS} < V_{DS}/2$) range, where the gate current is hole-dominated[34,35],

three damage species are found; interface states, trapped holes, and neutral electron traps[37,38,39]. However, most of the low gate voltage damage is not apparent immediately after stress. This is because the electron traps are neutral and the trapped holes mask the effect of the interface states. When stress at low gate voltage is followed by a brief electron injection phase, the neutral electron traps are filled and trapped holes neutralized, effectively exposing the damage[38]. It has been shown that low V_{GS} damage can occur for gate voltages below the threshold voltage of the MOSFET, and under certain conditions, damage for $V_{GS} < V_t$ can even predominate[40].

In the mid gate voltage($V_{GS} = V_{DS}/2$), the substrate current is maximum. Holes and electrons are injected together into the gate. S.K. Lai[36] in his MOS capacitor study found that interfacial trapped holes act as precursors to interface states when electrons are injected into the oxide and are trapped at this sites. This argument has been extended to interface state generation in MOSFET's[33] under this condition.

Under conditions of high gate voltages, the gate current is predominantly an electronic current. Significant damage has been seen to occur in this gate bias region[42]. Analysis has shown that in this region the damage is predominantly due to electron traps[41] which are filled by the hot electrons.

Figure 1.10 shows the different types of damage occurring in the gate voltage spectrum.

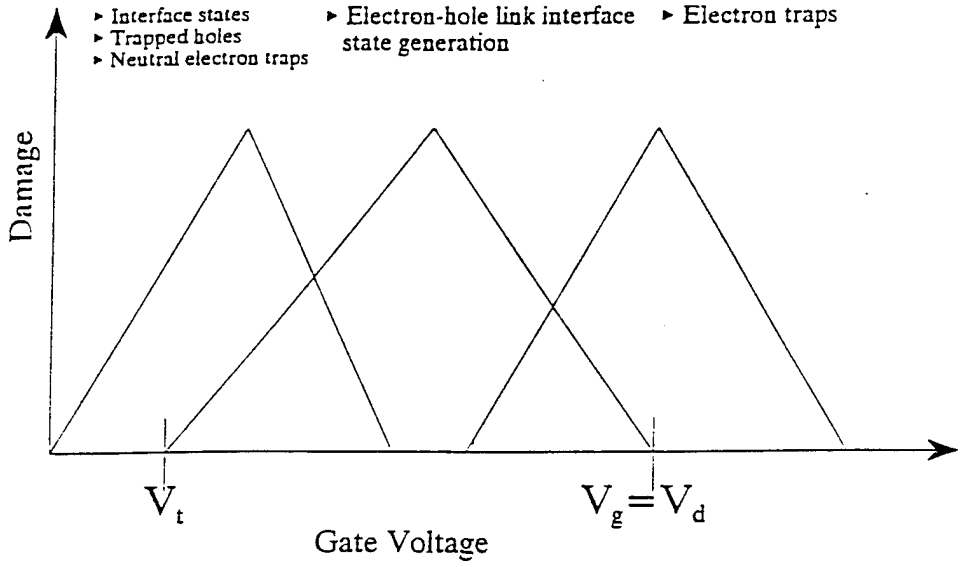


Figure 1.10 Representation of the different types of damage occuring in the gate voltage spectrum during DC hot-carrier stress at different gate voltages.

At low gate voltage, electron and interface states are created and hole trapping occurs; in the mid gate voltage region, interface states are the primary damage mode; and at high gate voltages, electron traps and a small amount of interface states are created.

1.4.2 Dynamic Stress Hot Carrier Damage

In practical MOSFET circuit application, the devices are subject to AC stress. The gate and drain voltages are functions of time. Thus the MOS devices are subject to

all the three damage mechanisms.

Several reports of AC stress experiments have described enhanced stress and/or substrate current effects associated with gate voltage transients in the present of high gate voltage. Mistry et al[43] combined the above three DC stress damage mode and proposed a AC stress damage function and proved that the three damage mechanisms,taken together, fully account for the so-call enhanced hot-carrier degradation.

1.5 Scope of This Dissertation

In this chapter, we have reviewed the history of studies of the hot carrier effects and the phenomena induced by hot carriers. We also introduced the recent understanding of the hot carrier induced damage. Following this, in chapter 2 we introduce some methods that have been used to reduce the hot carrier effect. A novel technique that uses the germanium implantation to reduce the hot carrier effects has been introduced. This technique shows great promise in reducing the hot carrier effects without effecting other electrical properties of MOS devices but has not been previously optimized. The focus of this dissertation is to investigate the effect of germanium implantation on MOS devices and to predict an optimum condition for minimizing device degradation. We would also like to study other neutral impurities such as carbon to see if they have the same hot carrier reduction ability as germanium. In the second part of chapter 2 we also review some properties of SiGe that have been discover by former researchers.

In chapter 3 we describe the experimental procedures and analytical techniques used in the various experimental investigations conducted during the course of this

research.

In chapter 4 the effects of germanium implantation on the MOS and MOSFET electrical properties are investigated. A significant reduction in avalanche injection gate current has been demonstrated. The hot carrier reduction due to germanium implantation has been observed in the hot carrier population versus energy curves. The hot carrier energy distribution curves show that the hot carrier energy is reduced with the germanium concentration. The effect of Ge implantation on the mobility of n-channel MOSFET has been studied. The effect of Ge implantation on the SiO_2 charge trapping property has also been investigated. A method to reduce the oxide charge trapping has been proposed. The effects of carbon implantation on MOS capacitor properties has been studied and compared with that of the germanium implanted sample. The hot carrier distribution of the Ge implanted sample obtained at liquid nitrogen temperature is presented. The result suggests the germanium implantation has a larger effect on the hot carriers effect at low temperature. Finally, we predict an optimum dose and energy for the germanium implantation for the MOS devices.

In chapter 5 we summarize our conclusions and suggest some directions for further research.

Chapter 2
Solutions for Hot Carrier Effect and Properties of SiGe

2.1 Introduction

From the first chapter, we know that the hot-carrier effect is one of the most serious problems posed by the continued shrinking of MOSFET dimensions into the submicrometer region. This effect arises from large electric fields that accelerate, or heat, inversion layer charge carriers. With the ever shrinking device geometries, this problem will increase as a limitation on the reliability of the devices, and therefore a lot of work has been devoted to the modeling of the hot-carrier phenomena and the physical mechanisms of hot carrier induced degradation. In the first part of this chapter, the various methods that have been used to reduce the hot-carrier effect will be introduced. The lightly-doped-drain (LDD) structure used to reduce hot-carrier effects deteriorates the current gain as the device dimension shrinks into the deep submicron region. Ge implantation into the channel of MOSFET to reduce the hot carrier effect has been recently discovered[21]. In order to gain some insight into the Ge process, some characteristics observed by former researchers will be introduced in the second part of this chapter.

2.2 Solutions for Hot Carrier Effect

In this section various solutions for the hot carrier effect are reviewed.

2.2.1 Drain Engineered Structure

Because hot carrier effects are driven by the high electric field near drain, various

MOS structures with specially designed drain regions have been proposed to reduce the peak electric field[80]. The lightly doped drain (LDD) structure was the most successful structure to reduce hot carriers. A cross section of a lightly doped drain-source[44] structure is pictured in figure 2.1. In the LDD structure, narrow, self aligned, n^- regions are introduced between the channel and the n^+ source drain diffusion. The reduction in electric field intensity due to the LDD structure is clearly illustrated in Fig 2.2. The electric field at the Si-SiO_2 interface as a function of distance along the channel near the drain is plotted for a conventional and an LDD device. The electric field in the conventional device peaks approximately at the metallurgical junction and drops quickly to zero in the drain because no field can exist in the highly conductive n^+ region. On the other hand, the electric field in the LDD device extends across the n^- region before dropping to zero at the drain. For a given voltage the areas under the two fields curves are equal, so the peak field in the LDD device must be lower than in the conventional device. With the decrease in electric field, the breakdown voltage increases and impact ionization is reduced in the LDD structure. However, when a lightly doped region is introduced between the channel and drain, it introduces a series resistance. As the channel is scaled below 0.5 μm, the resistance due to the LDD structure is not negligible compared to the channel resistance and the current and gain decrease[45]. Later research[46,47] also shows that the LDD structure is more susceptible to hot electron damage due to localized interface states and trap charge located above the lightly doped drain. For further reduction in the channel length, some other approach has to be made to avoid the series resistance problem caused by the LDD structure.

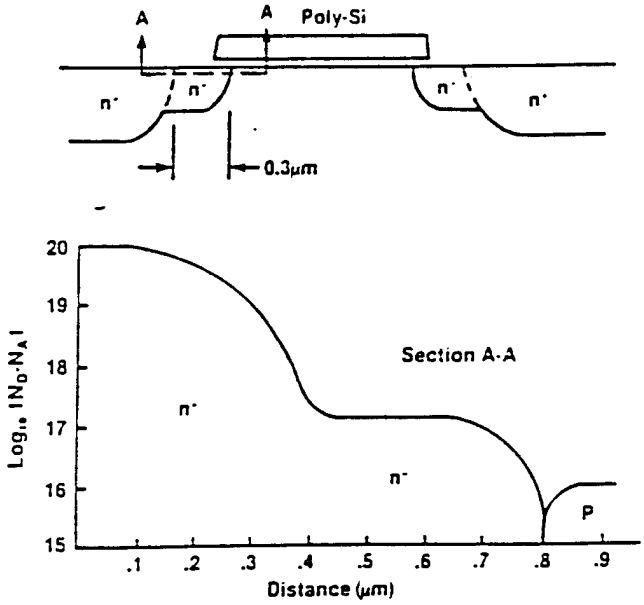


Figure 2.1 LDD structure. The self-aligned n^- regions between the channel and the n^+ source and drain diffusion is the unique feature of the LDD structure.

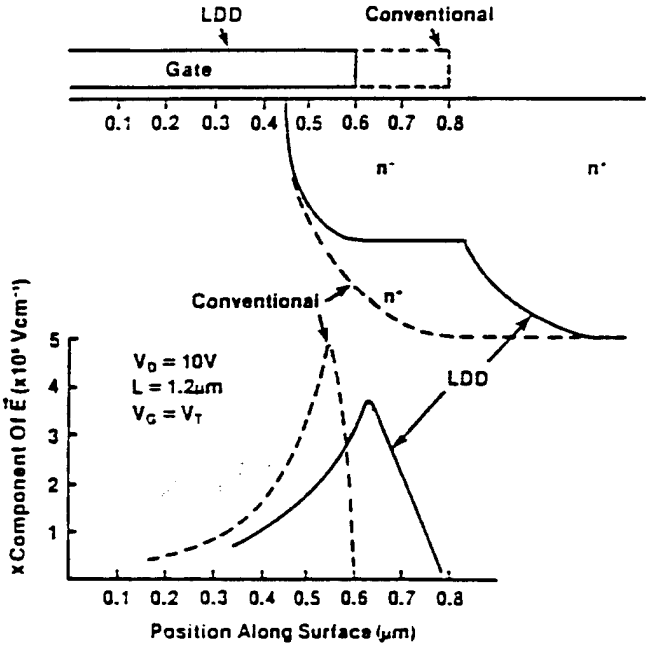


Figure 2.2 Magnitude of the electric field for the LDD and conventional devices at the Si-SiO_2 interface as a function of distance.

2.2.2 Hot Electron Hardened of Insulating Layer

Because the device degradation is caused by the hot carriers injected into the gate oxide near the drain, one approach is to decrease the charge trapping in insulator.

T.P Ma et al[49,50] found that appropriate addition of fluorine to the oxide gives rise to a significant reduction in the hot-electron induced interface states. The results are shown in figure 2.3. They claimed that the bond strain distribution near the Si-SiO_2 interface may be decreased by the presence of F in the SiO_2.

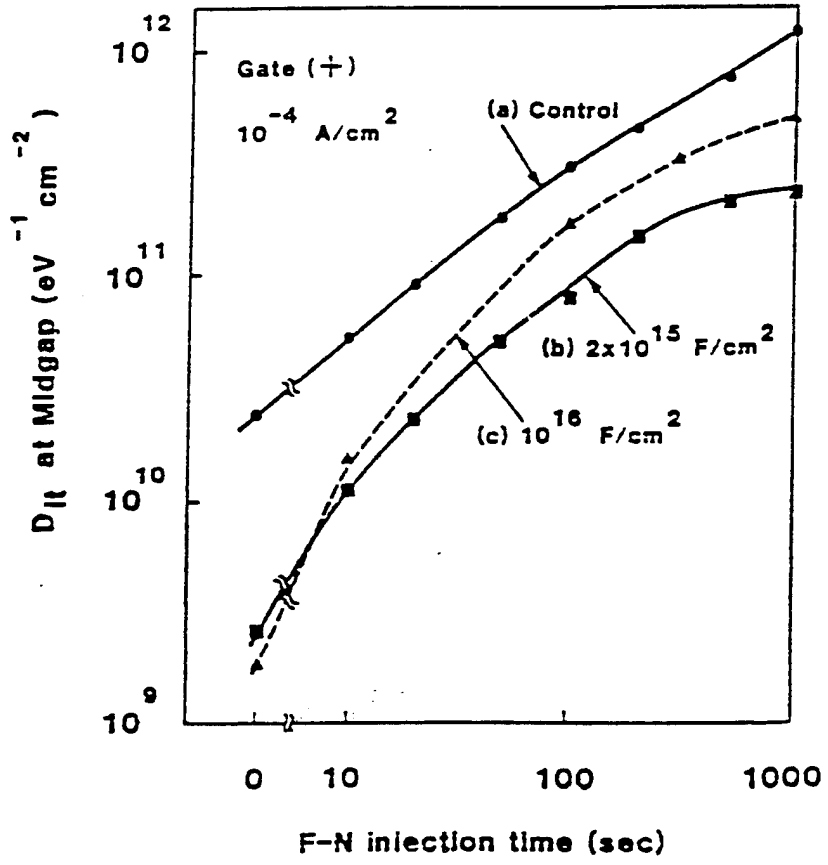


Figure 2.3 Increase of interface trap density for three sets of MOS capacitors as a function of F-N electron injection time. Electron were injected from silicon substrate as a constant current of 10^{-4} A/cm^2. (a) Control, (b) 2 × 10^{15} F/cm^2, and (c) 10^{16} F/cm^2.

Young and D. Xie[51] found that fluorine implantation can reduce slow interface states and eliminate the turn-around effect during avalanche injection as shown in figure 2.4.

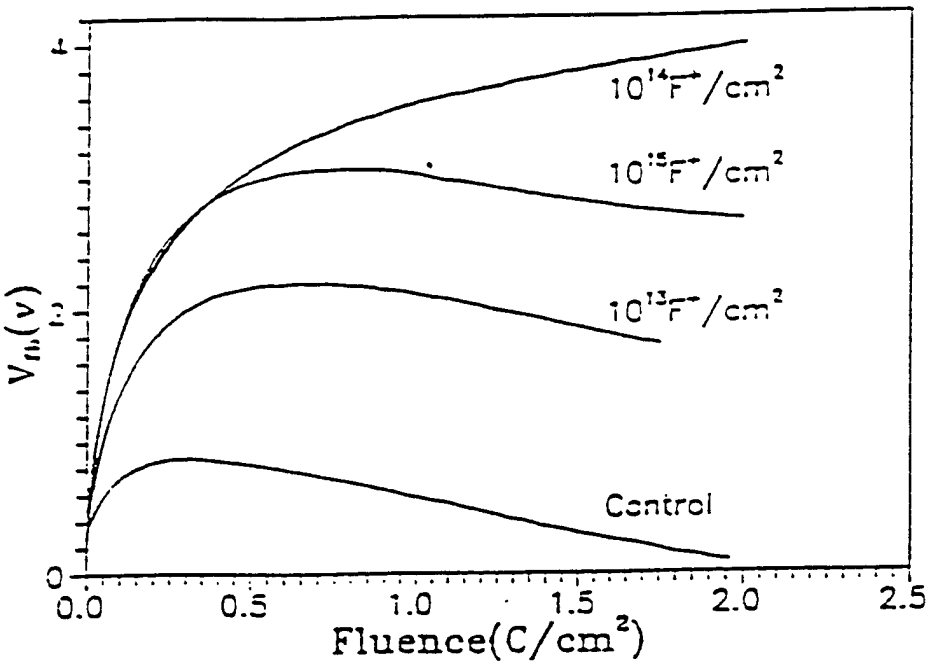


Figure 2.4 Avalanche electron injection curves of control and fluorinated oxide at room temperture.

R. Jacoodine and D. Kouvastsos[52] observed the reduction of as-grown interface state densities in MOS (figure 2.5) as a result of the addition of fluorine. They claim that fluorine can react with interface dangling bonds and passivate the interface trap center.

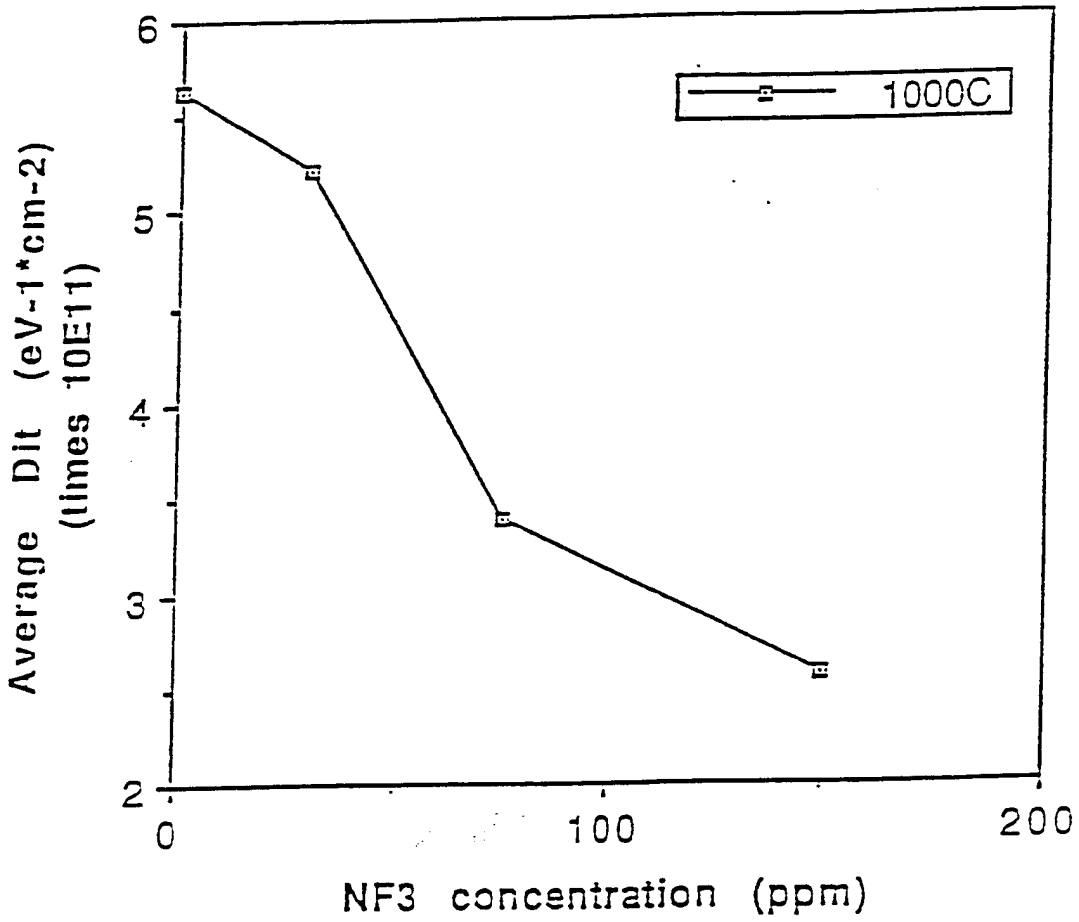
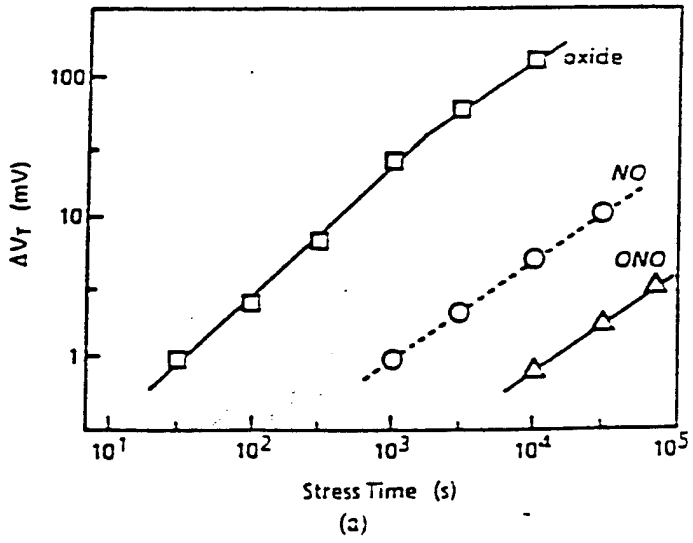


Figure 2.5 Average interface trap density against NF_3 concentration.

The incorporation of nitrogen at Si-SiO_2 interface to reduce the hot carrier effect has also been discovered. Reoxidized-nitride oxide (RNO's)[53-56], thermally nitrided in NH_3, have excellent characteristics towards hot-carrier effects with reduced interface state generation and act as a barrier towards impurity penetration into the SiO_2; However, electron trapping is inherent in nitride oxide due to hydrogen, and reoxidation is needed to reduce H concentration[57]. Rapid thermal processing in a nitrous oxide (N_2O) ambient[58-60], essentially free of hydrogen atoms, results in oxides that are highly resistant to hot-carrier effects with reduced electron trapping[61]. Figure 2.6 shows the reoxidation of NO reduces both V_{th} and g_m degradation.



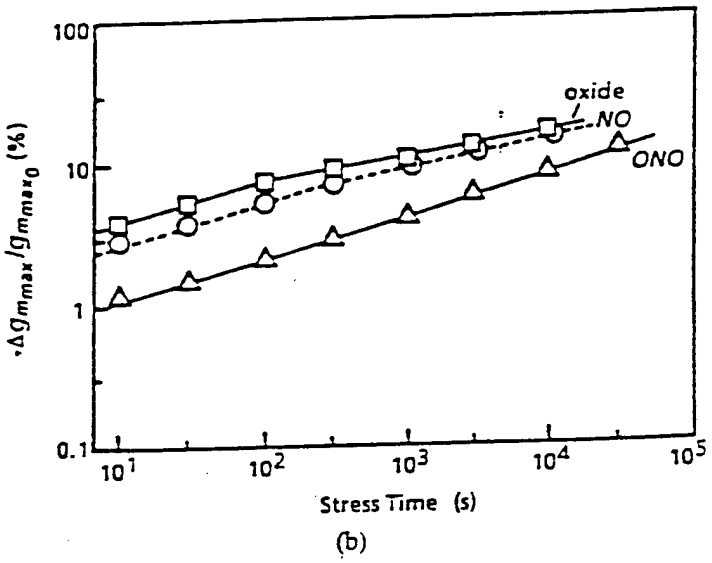


Figure 2.6 (a) V_T shift (b) g_m degradation as a function of stress time for 0.8 μm MOSFET's with a pure oxide, NO, and ONO. The reoxidation reduces both V_T shift and g_m degradation remarkably.

2.2.3 The Reduction of Voltage

The reduction of operating voltage is another approach to reduce the high electric field. Some companies have accepted the 3.3 V standard. Recently, the state of the art CMOS operates at 2.5 V[48]. Generally, the applied voltage has not been decreased as much as the channel length, so hot carrier degradation has increased.

2.2.4 Ge Implantation

Ng et al[6] recently proposed a new technique to suppress hot electron effects. The technique is based on the introduction of an additional scattering mechanism with mean free path value larger than that seen by the majority of the channel carriers such that the MOSFET current is not modified, but smaller than that seen by the lucky hot carriers such that they lose energy through added scattering.

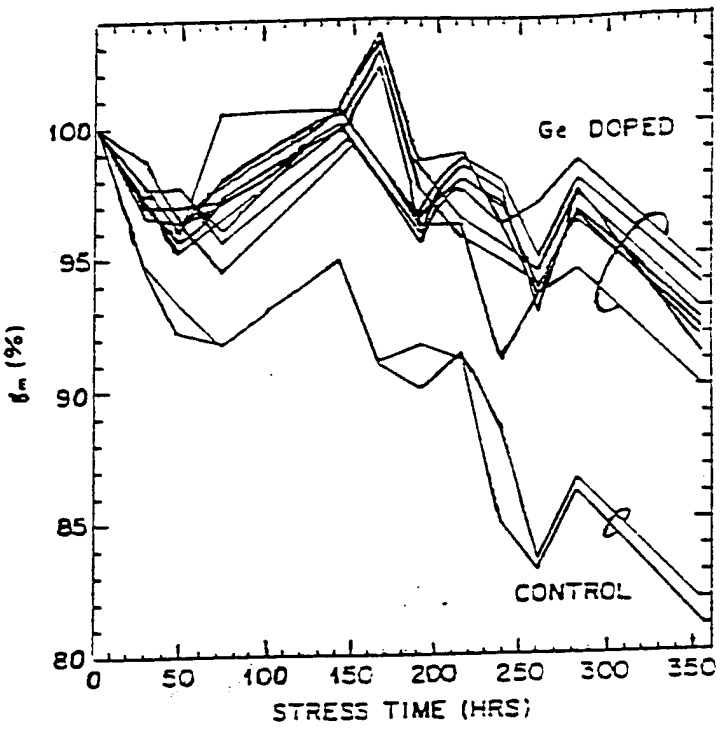


Figure 2.7 Transconductance g_m in the triode region relative to the initial value as a function of stress time for the control devices and Ge-doped structures.

They found that the introduction of germanium into the channel of the MOSFET can reduce hot carrier effects without changing the electrical properties of the device. Their results are shown in figure 2.7. This technique shows promise in reducing the hot-carrier effects and has not yet been optimized. In this dissertation the effect of germanium implantation on the MOS capacitor and MOSFET will be investigated and a optimum dose will also be suggested.

2.3 Some Properties of SiGe

The lattice mismatch between silicon and germanium is only 4.17% at room temperature, and Si and Ge are completely miscible over the entire compositional range and give rise to a continuous series of alloys with a diamond cubic crystal structure. Since fairly homogeneous single crystal or polycrystalline specimens of arbitrary composition can be prepared, the SiGe alloy is now widely used in silicon technology to improve the characteristics of semiconductor devices. Some of the properties of SiGe alloy will be presented next.

2.3.1 Bandgap Narrowing

$Si_{1-x}Ge_x$ alloys have a smaller band gap than silicon, principally because of a larger lattice constant and altered lattice constituents. The energy gap value as a function of Ge content according to Braunstein et al is shown in figure 2.8[63].

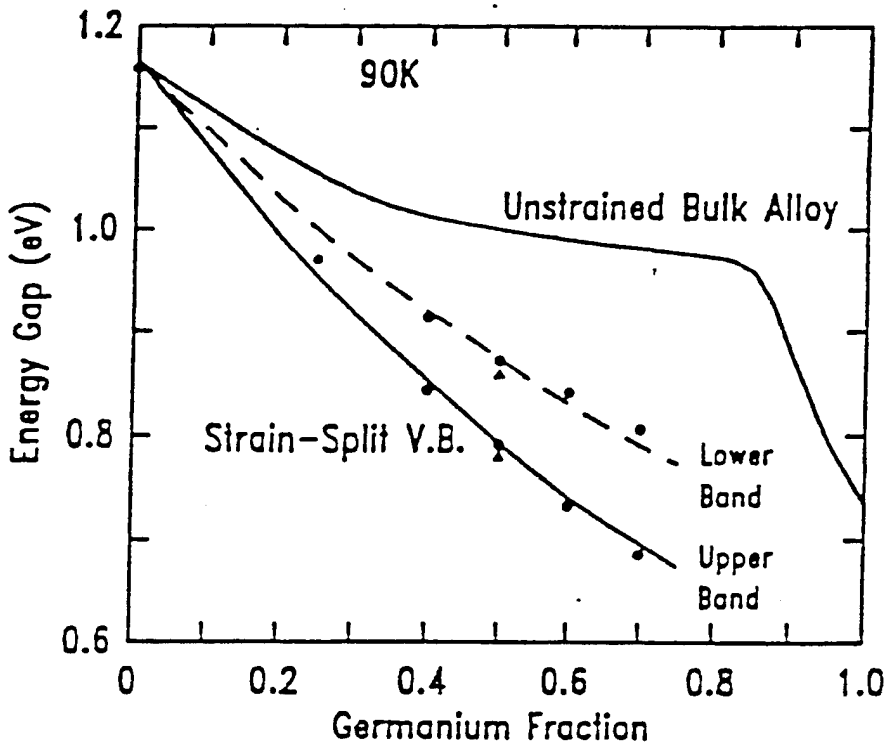


Figure 2.8 Bandgaps for unstrained bulk $Si_{1-x}Ge_x$ alloys and psedo-morphic $Si_{1-x}Ge_x$ alloys.

This ability to change the bangap has led to the manufacture of hetrojunction bipolar transistors (HBT's) with SiGe base and modulation-doped field-effect transistor (MODFET's)[64,65], resonant tunneling diodes[66,67,68] ,and optoelectronic devices, such as a Ge p-i-n photodetector on Si substrate[69], pseudomophic strained layer super lattice p-i-n photodetectors[70], avalanche photodetectors[71], long wavelength photoconductive detectors[72], and bipolar inversion channel field effect transistor (BICFET's).

2.3.2 Electron Mobility

The low field electron mobility in intrinsic $Si_{1-x}Ge_x$ has been experimentally

determined and calculated from band theory[73]. L.E. Kay et al[74] used Monte Carlo (MC) simulation to obtain the low-field electron mobilities. The results are shown in figure 2.9.

Figure 2.9 shows that in a doped SiGe alloy the fall off in mobility become smaller with increasing x. When doping density reaches 10^{20} cm^{-3} , mobility is virtually independent of germanium concentration x.

To explain this effect, we know that the scattering mechanisms in SiGe includes alloy scattering caused by germanium and ionized impurity scattering caused by the doping atoms, thus the mobility can be written as,

$$\frac{1}{\mu} = \frac{1}{\mu_{alloy}} + \frac{1}{\mu_{imp}}$$

where μ_{alloy} is the alloy scattering-limited mobility, μ_{imp} is the impurity mobility.

In the intrinsic case the scattering mechanism is dominated by alloy scattering, so the carrier mobility (μ_{alloy}) decreases with the germanium concentration. However, as the impurity concentration increases, the domination of alloy scattering decreases and the mobility is not sensitive to the germanium concentration. The concentrations used in the experimental portion of this work are smaller than the required to reduce the mobility.

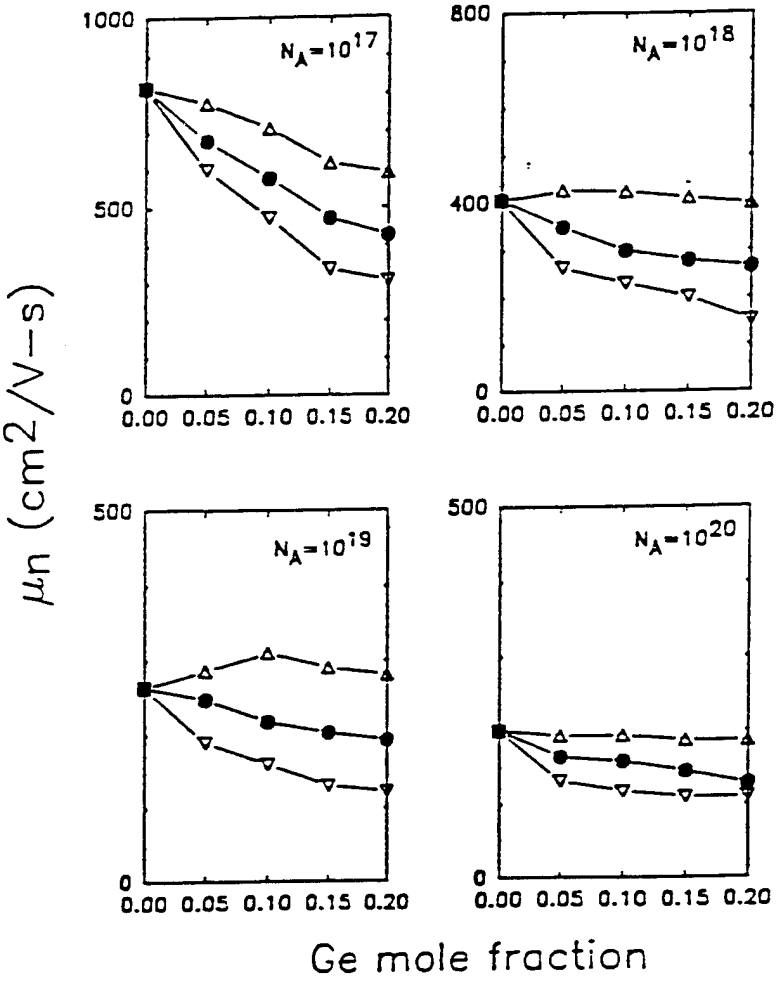


Figure 2.9 MC calculated electron mobility in p-type $Si_{1-x}Ge_x$ as a function of x and acceptor concentration N_A[74].

2.3.3 Electrical Properties Improved by SiGe

Germanium doping in silicon has been shown to lower the number of silicon point defects in the wafer, and thereby reduce the diffusion of dopants[75]. Pfiester and Griffiner[75] showed that the normal phosphorus kink and tail are absent when high concentration of phosphorus is co-diffused with germanium. Pfiester et al[76] used the germanium implantation to reduce the diffusion of source and drain dopant. They found the short channel effect (Figure 2.10) of the MOSFET is improved with germanium implantation because Ge implantation can result in shallower source-drain junction.

C.R. Selvakumar and Bruce Hecht[77] used high dose germanium implantation to manufacture the SiGe channel MOSFET. Their SiGe MOSFET's show significant higher performance than Si-channel MOSFET's.

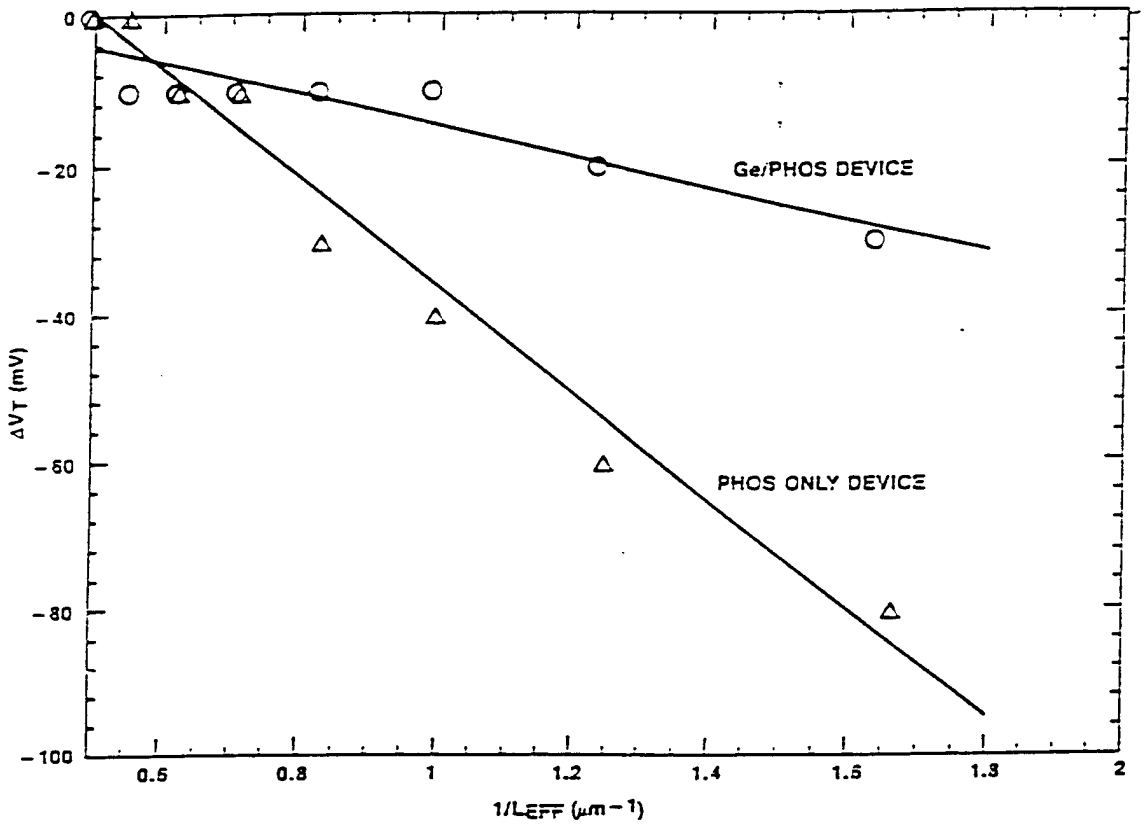


Figure 2.10 Threshold-voltage shift as a function of the inverse electrical channel length[77].

Chapter 3

Experimental Procedure and Analytical Techniques

3.1 Introduction

The techniques that have been used in this dissertation will be presented in this chapter. The experimental procedures utilized are shown in figure 3.1. The metal-oxide-silicon (MOS) capacitor has been used as the principal structure for the study of the effects of germanium implantation on the electrical properties of the MOS system; its simplicity and the capability for direct measurements and monitoring of integrated circuits make the MOS capacitor a suitable structure for the extraction of several quantities, such as, interface state density, oxide trap charge, and hot carrier population. After the understanding of the basic properties, an optimum implantation energy and dose for the Ge will be predicted. This implantation condition will then be used to make a MOS field effect transistor (MOSFET). The current voltage (I-V) method will be used to evaluate the carrier mobility of the MOSFET's.

3.2 Measurement for MOS Capacitor

3.2.1 Review of Charges in MOS

The two terminal metal-oxide-silicon (MOS) capacitor is both the simplest of MOS devices and the structural basis for all MOS devices. Because of the ease of fabrication and the functional simplicity, any change in processing that improves the

electrical properties of the MOS capacitor results in the same improvement on the actual MOSFET device.

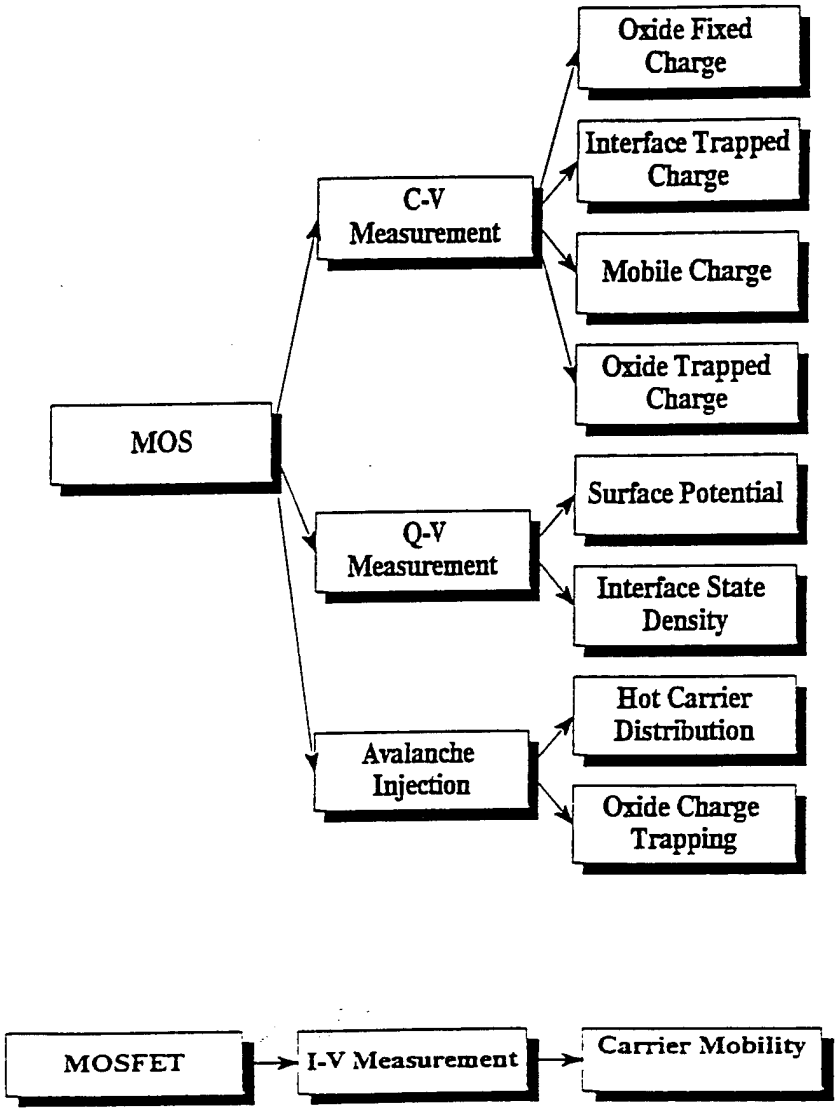


Fig. 3.1 Flow chart for experiments and parameters extraction.

We use the MOS capacitor to study the fixed charge, interface state density, oxide charge trapping and hot carrier effects. There are four types of charges in MOS[81] illustrated in figure 3.2 which cause the deviation of MOS from ideal.

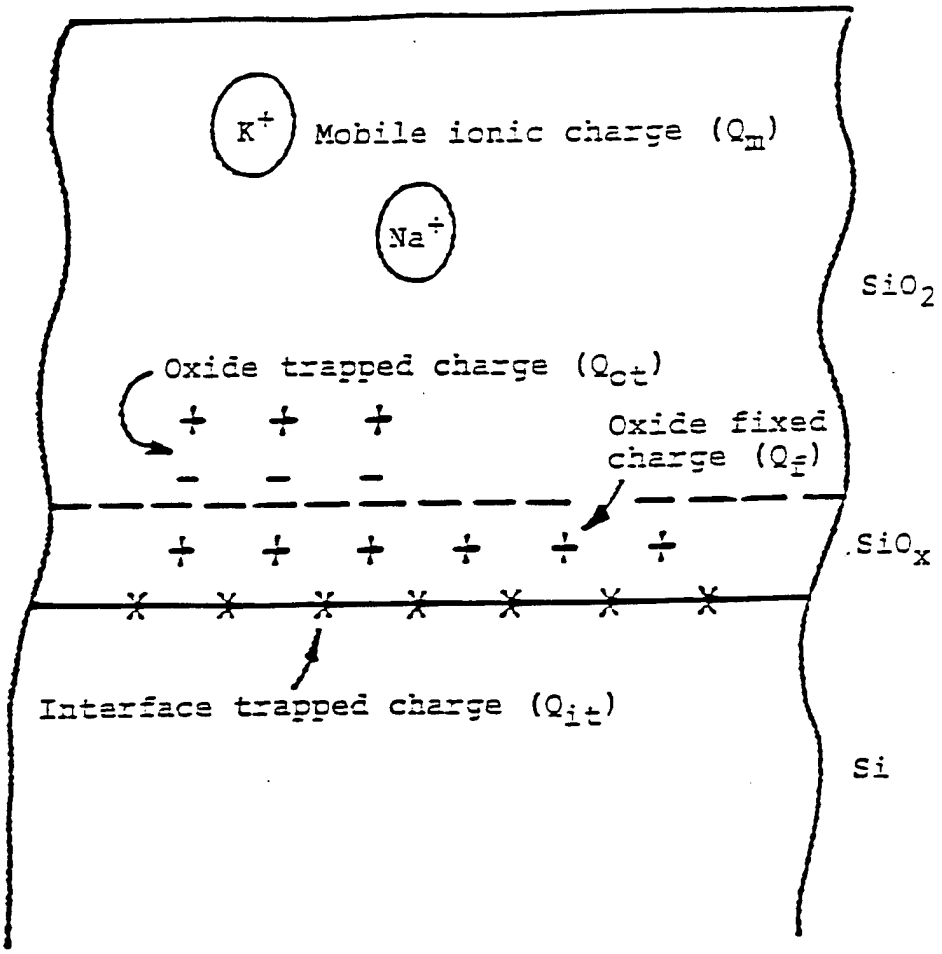


Fig. 3.2 Categories and location of oxide charge in the MOS system.

The bulk trapped charge Q_{ot} consists of electrons and holes which have been captured by traps in the oxide bulk. The fixed oxide charge Q_f which resides within the oxide very close to the oxide-semiconductor interface is due to excess ionic silicon that has broken away from the underlying silicon and is waiting to react in the vicinity of the Si-SiO_2 interface when the oxidation process is abruptly terminated. The mobile ion charge Q_m in the oxide is due to alkali ions, especially sodium ions. The sodium ions are inadvertently introduced by chemical reagents, the hands of laboratory personnel and the glass in the oxidation apparatus. The interface (Q_{it}) traps primarily arise from unsatisfied chemical bonds or so called "dangling bonds" at the surface of semiconductor. Various techniques are useful to evaluate the non-ideality of our samples. The techniques include the high frequency capacitance-voltage (C-V) method, the charge-voltage (Q-V) technique and the avalanche injection (AVI) technique. A new Q-V technique has been developed in our laboratory and used in this dissertation is an accurate method to evaluate the Si-SiO_2 interface. We will explain this technique in detail.

3.2.2 The High Frequency C-V Technique

The high frequency C-V ramp method[82] has been commonly used in the industry for quick scanning of the charge characteristics of MOS capacitors. The schematic of the C-V measurement used for carrying out the C-V electrical characterization of our capacitors can be seen in figure 3.3. It consists of an personal computer controlling the system, a stage to hold the wafer, a Keithley data interface and a PAR model 410 C-V plotter with built-in voltage ramp generator and capacitance measurement system. As the gate ramp voltage across the oxide dielectric of the capacitor is slowly varied, the 1

Mhz small saw-tooth test signal is superposed on ramp voltage.

By comparing the experimental C-V curve with the ideal C-V curve, we can derive useful information about the electrical properties of MOS system as shown in figure 3.4. The fixed oxide charges produce rigid shifts in the flat band voltage (V_{fb}) which can be used to determine the charge density. The mobile ions present would move, particularly at higher temperature, in response to a gate voltage, thus changing the flat band voltage. The energy states of interface traps are distributed throughout the silicon band gap. Thus, as the gate voltage changes the Fermi-level, the occupancy status and therefore the charge state changes. As a result, the magnitude of the interface traps charge depends on gate voltage. The interface traps will thus stretch out the C-V curve.

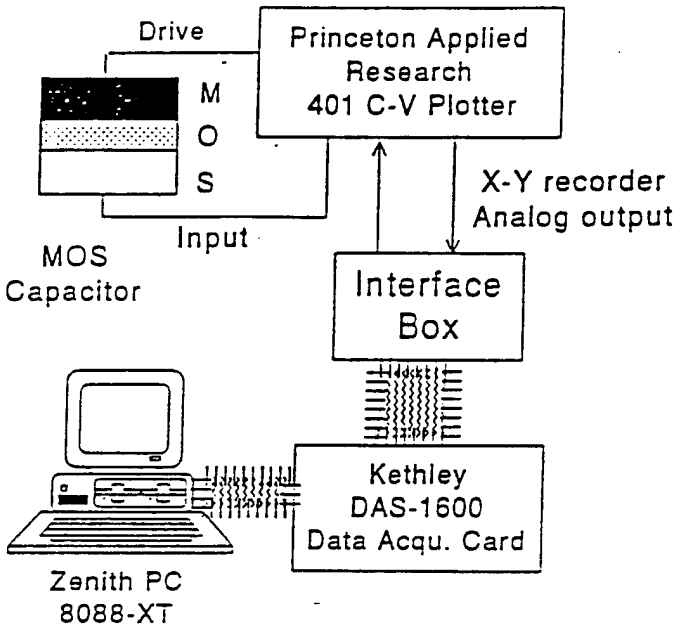


Figure 3.3 High frequency C-V measurement set-up.

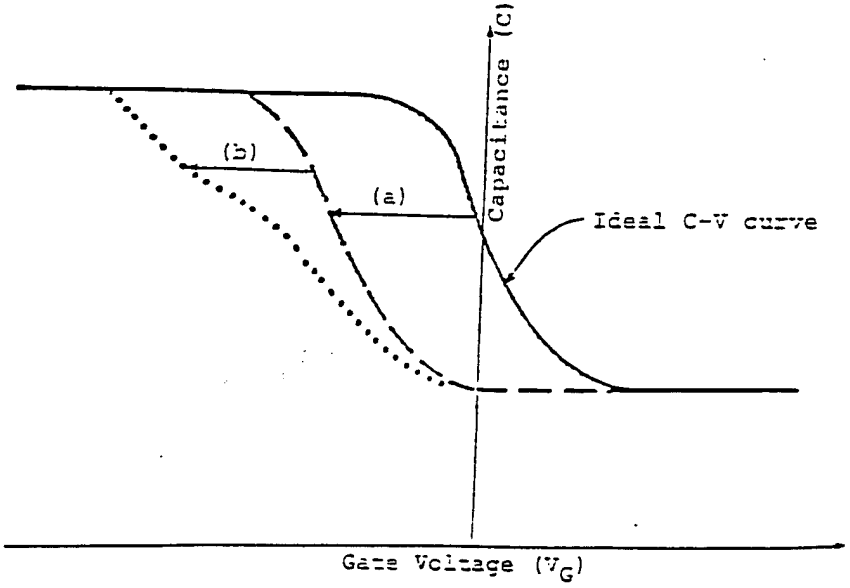


Fig. 3.4 High frequency C-V curve for a MOS capacitor with a p-type substrate. (a) Rigid shift and (b) Stretch-out effect.

3.2.3 Q-V Technique

3.2.2.1 Introduction

A more accurate and direct method of extracting data suitable for the determination of the interface trap density has also been developed and utilized in our lab.[85]. It is the charge-voltage (Q-V) method, so-called because it is based on direct static measurement of the charge of the MOS capacitor for given values of the gate voltage. The Q-V technique was originally proposed by Ziegler and Klausmann[83] and has been extensively discussed by Nicollian and Brews[84]. This technique has been used by Nicollian and co-workers in numerous subsequent publications. Briefly the technique consists of placing a known ultralow leakage, voltage independent, reference capacitor (C_i) in series with the MOS capacitor. A very low leakage voltmeter, which in our case is an electrometer used in unity gain configuration, to measure the voltage across the reference capacitor. A precision measurement of the electrometer output voltage is made. The measured voltage gives a measurement of the change of charge in the circuit. Since this capacitor is in series with the oxide capacitance, the change in charge across the oxide capacitance will be equal to the charge measured by the electrometer. If the oxide capacitance is known, a simple calculation gives the change in voltage developed across the oxide. The interface potential is equal to the gate voltage less the oxide voltage. This technique makes it possible to calculate the surface potential (ψ_s) verses applied voltage (V_G), allows a higher accuracy in determination of the MOS interface parameters and makes possible the derivation of energy distribution of interface state density over a large part of the energy gap. Moreover, since it is a point by point

technique it is particularly suitable for used with computer. A major advantage of the Q-V technique as compared with other techniques is that it does not depend on the semiconductor doping concentration. Frequently, this concentration is not accurately known and it is a major concern in practical cases where the concentration changes with depth in the semiconductor. One problem consists of an unknown constant involved. In practice when the measurement is started, the reference capacitor is shorted to ground so the initial measured voltage is zero. At this point the interface potential is not known. We can, however, measure the changes in the interface potential as the applied gate voltage is varied. A simple means for determining this unknown constant has been used. Our contribution is a new means to determine this constant.

3.2.2.2 Experimental Set-up

The experimental setup we have used for the Q-V measurements is shown in figure 3.5. It is based on the basic circuit for the Q-V technique; however, it is a computer controlled system with software that controls the system hardware and evaluates the results. A voltage independent capacitor C_i is connected in series with the MOS capacitor. The capacitance C_c is in parallel with the MOS capacitor is the parasitic capacitance of the wafer holder and cables.

We find C_c to be negligible (0.1 % of C_i) when we calibrate the system. A twelve bit digital analyzer (D/A) converter supplies the circuit input step voltage V_a over the range to $\pm$ 5 V. A 2$\times$ buffer amplifier is connected to the output of the D/A converter to increase the range of V_a to $\pm$10 V. The voltage (V_i) across C_i is measured by a Keithley 616 electrometer which has an input impedance greater than 2×10^{14} Ω. The

output voltage of the electrometer is captured by a 16-bit A/D converter which gives us an accuracy of 0.3 mV. The measurement procedure is controlled by a computer program. First, the 12-bit D/A converter is activated and the digital signal for the desired V_a is sent from the computer to the D/A converter. A delay loop is used to generate the waiting period which is necessary for the system to became stable. Then the 16-bit A/D converter is activate to convert the analog signal from the electrometer.

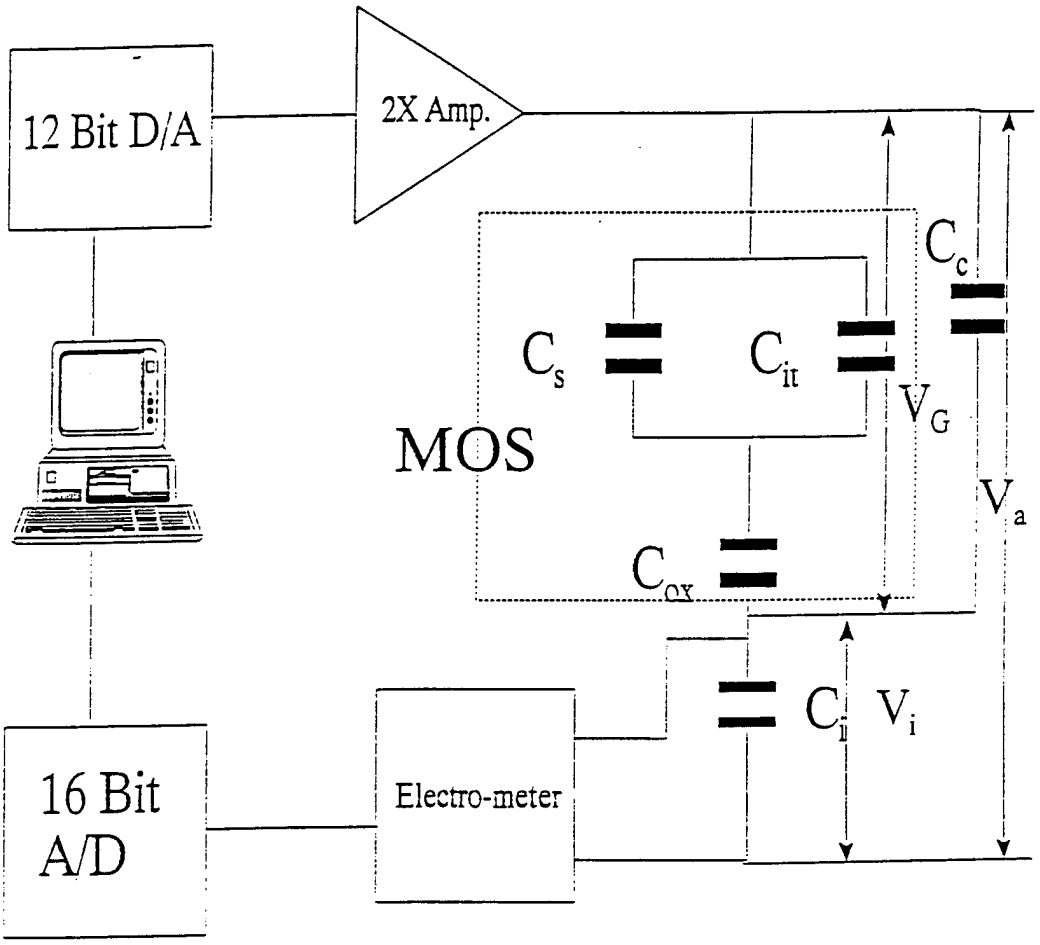


Fig. 3.5 Q-V measurement set-up.

3.2.2.3 Parameter Extraction

The voltage V_G across the MOS capacitor is given by

$$V_G = -(V_a - V_i) \tag{3.1}$$

where V_a is the applied voltage and V_i is the voltage across the voltage independent capacitor C_i. A typical plot of V_i vs. V_G is shown in fig. 3.6.

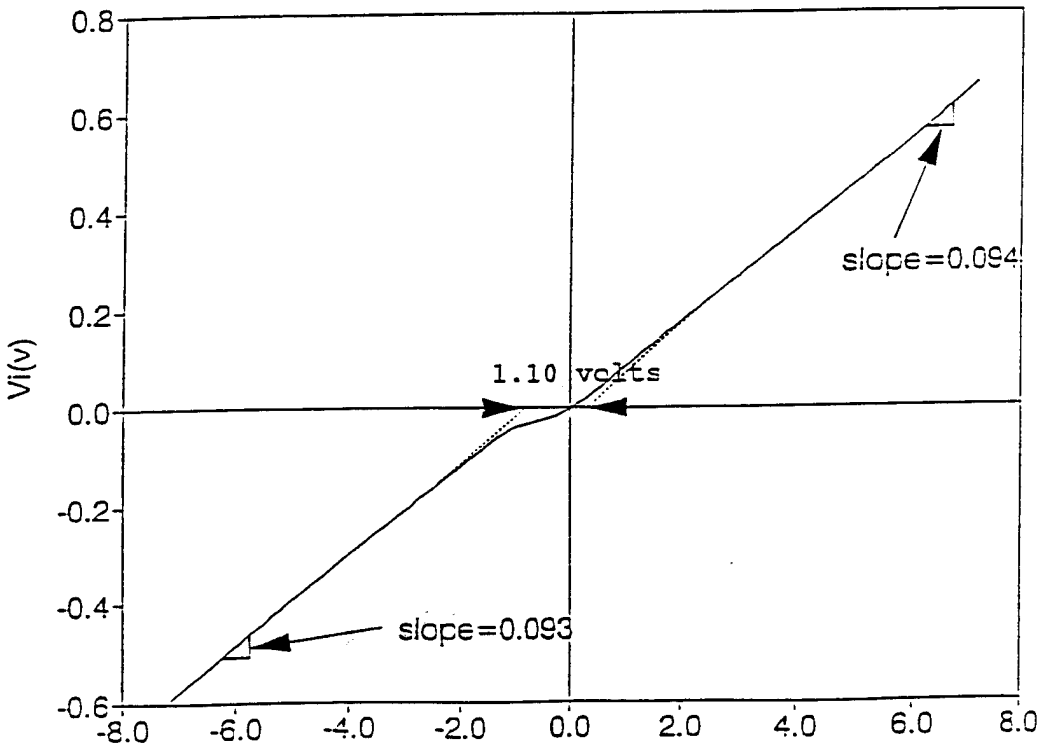


Fig. 3.6 Voltage across C_i (V_i) versus Gate voltage (V_G) curve.

The charge Q_G which flows into the gate electrode is

$$Q_G = -C_i V_i - C_c V_G \tag{3.2}$$

Because C_c is negligible compared to C_i, we ignored the second term of Eq.(3.2) in our calculation. The surface potential ψ_s is the difference between the V_G and the voltage drop across the oxide which is equal to Q_G/C_{ox} :

$$\psi_s = V_G - \frac{Q_G}{C_{ox}} + \psi_o \tag{3.3}$$

where ψ_o is the surface potential at the voltage $V_G=0$.

To determine ψ_o, we assume that in accumulation the interface potential is at the edge of silicon valence band (for p-type silicon) and for strong inversion the interface potential is at the edge of silicon conduction band. The mid point of these measurements is taken as the mid gap point. In our plots we use this midgap potential, which is taken as zero, as a reference. This calibration is independent of the silicon doping profile and only requires a knowledge of the effective reference capacitance which is the sum of the reference capacitance and the input capacity of the electrometer. The mid gap point is different from the usual reference which is the flatband point. This difference is given by the location of the Fermi level in the silicon relevant to mid gap for constant doping concentration. If this concentration is not constant then the flatband concept can not be applied.

To be able to calculate the surface potential, it is necessary to know the oxide capacitance. This can be measured with a high frequency bridge with the sample in accumulation, or by the technique describe below:

The derivative of eq.(3.2) with respect to V_G is given by:

$$\frac{\partial Q_G}{\partial V_G} = C_i \cdot \frac{\partial V_i}{\partial V_G} \tag{3.4}$$

In accumulation strong inversion $\partial Q_G/\partial V_G = C_{ox}$, so from Eq.3.4 the slope of the line in Fig.3.6 gives the oxide capacitance. The interceptions of these lines with the gate voltage axis should be displaced by the band gap using the simple picture described. We obtain a value of 1.1 V for the displacement, which is certainly close to the known value for the energy gap in silicon. This agreement supports the technique we have used to obtain the unknown constant. The plot of interface potential versus gate voltage (Fig. 3.7) indicates that the interface potential is not completely clamped at the band edges but there is a small increase in magnitude. This increase is due to an increase in the band bending in the semiconductor occurring in strong inversion or strong accumulation. This leads to a possible source of error in the technique described above. If the band bending is reasonably symmetrical for the accumulation and the inversion cases, then this would not introduce an error. We use complementary points to make a first-order correction for band bending in order to reduce the error. This concern becomes much more important as the oxide thickness decreases where the band bending becomes more comparable to the applied gate voltage. For thin oxides a more refined correction should

be made.

The measured values for the surface potential can be compared with the theoretical results using Kingston-Neustadter theory[86] as shown in fig 3.8. At a given surface potential, there is difference, V_G, of gate voltage between the experimental and theoretical curves. This difference is caused by the interface state charge, fixed charge in the oxide, and work function difference between metal gate and SiO_2.

$$C_{ox}\Delta V_G=\Delta Q=Q_f+Q_{it}+\omega \tag{3.5}$$

where Q_f is the fixed charge in the oxide, Q_{it} is the interface state charge, and ω is a constant due to the work function difference.

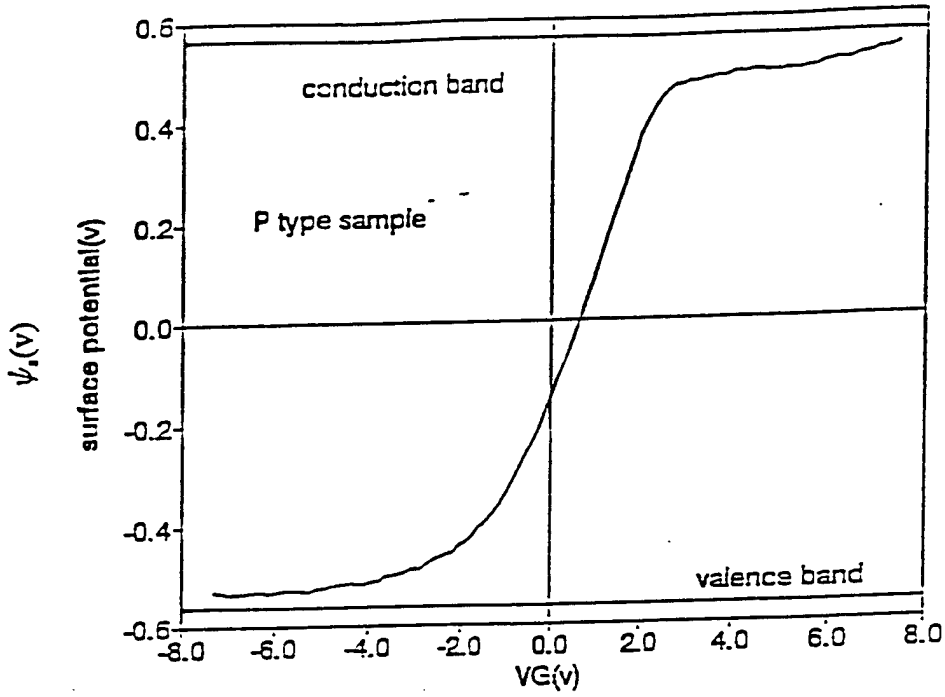
Because Q_f and ω are independent of the surface potential, taking derivative of Eq. 3.5 with respect to ψ_s we obtain:

$$\frac{\partial Q_{it}}{\partial \psi_s}=-\frac{\partial(\Delta Q)}{\partial \psi_s} \tag{3.6}$$

The interface state is given by

$$D_{it}\equiv\frac{1}{qA}\times\frac{\partial Q_{it}}{\partial \psi_s} \tag{3.7}$$

where A is the area of the gate and q is the magnitude of the electronic charge. A typical interface state density vs surface potential curve is shown in Fig 3.9.



(a)

(b)

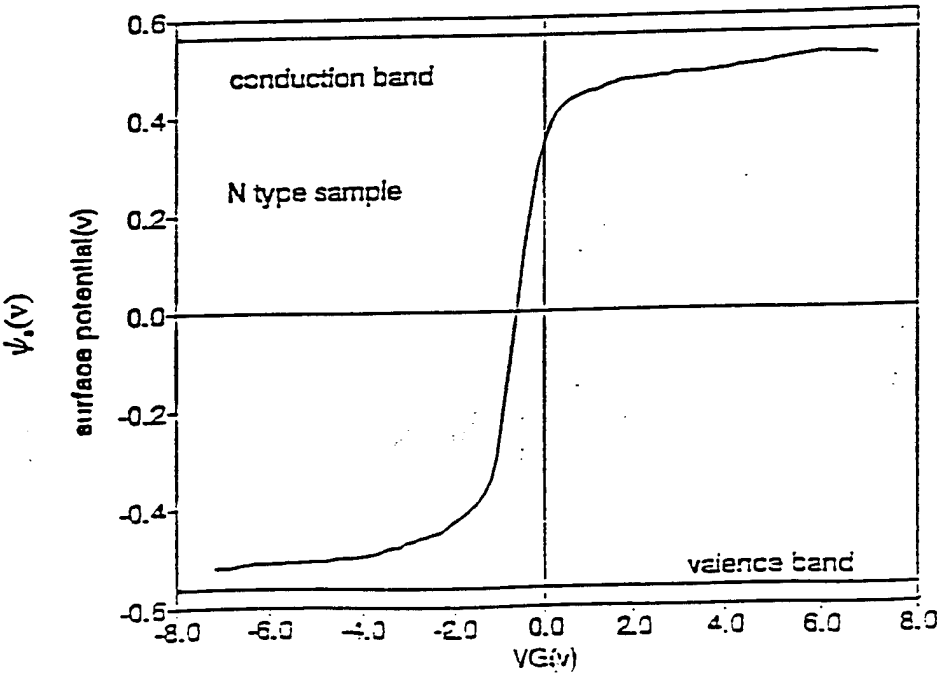


Fig. 3.7 Typical Surface potential (ψ_s) versus Gate voltage (V_G) curve. (a) p-type sample, (b) n-type sample.

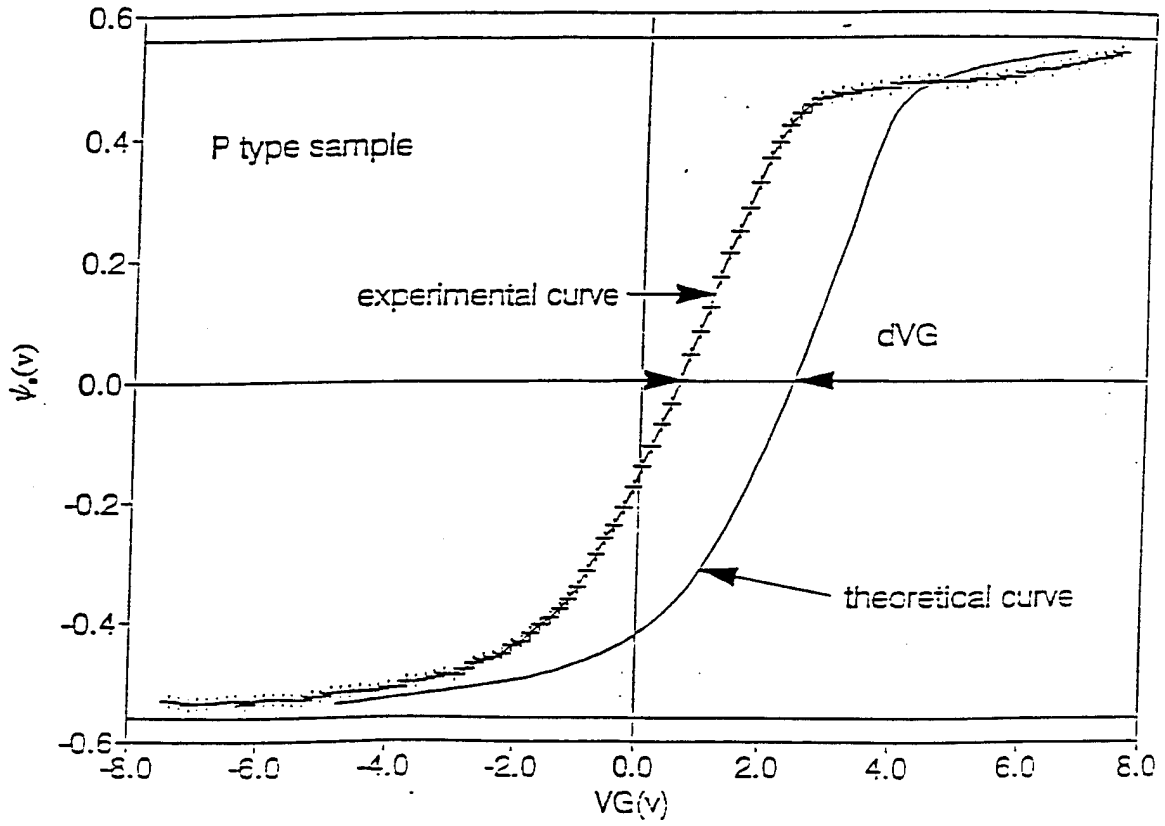


Fig. 3.8 Measured and theoretical ψ_s versus V_G curve.

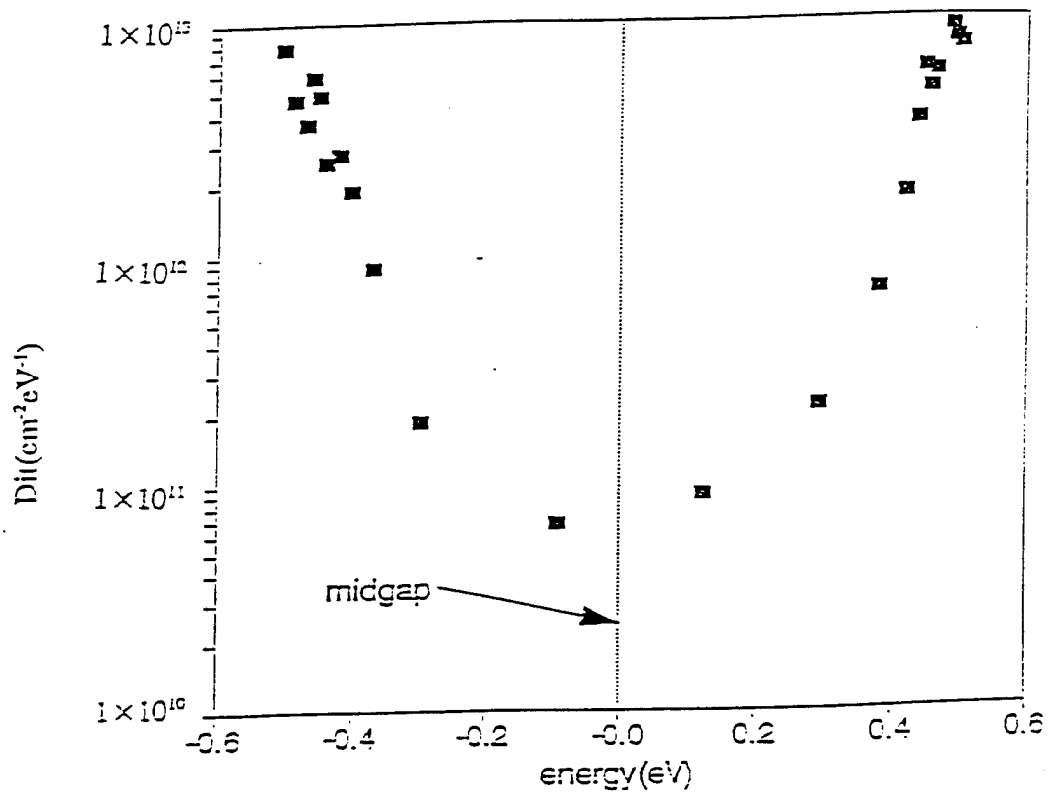


Fig. 3.9 Typical interface state density vs. surface potential curve.

3.3 Avalanche Injection Technique

3.3.1 Introduction

Avalanche injection has been described respectively by Nicollian[87] and Young[88] as a means to induce a current flow in the oxide. Under an avalanche condition in the silicon, the MOS capacitor is driven to deep depletion and minority carriers in the silicon substrate are accelerated by the applied electric field. These hot carriers have sufficient energy for impact ionization to occur. Thus, electron-hole pairs are created in silicon surface depletion layer. Some of the electrons or holes have enough energy to surmount the interfacial barrier and enter the SiO_2 to form a current. Generally, electrons are injected when the substrate is p-type and holes when the substrate is n-type.

The injection process is illustrated in figure 3.10. Figure 3.10(a) shows one cycle of the electric field across the oxide. Figure 3.10(b)~(d) show band bending in both oxide and silicon at various times during ac cycle. At time t=0 (Fig 3.10b), the band are assumed to be flat. Then the bands begin to bend the silicon surface tends toward inversion. Deep depletion is reached at time $t=t_1$ (Fig 3.10c). Band bending increases with further increase in field until avalanche breakdown ($3\sim5\times10^5$ V/cm), initiated by thermally generated carriers, occurs at silicon surface. The silicon remains in avalanche breakdown condition during the time interval t_A shown in Fig 3.10(a).

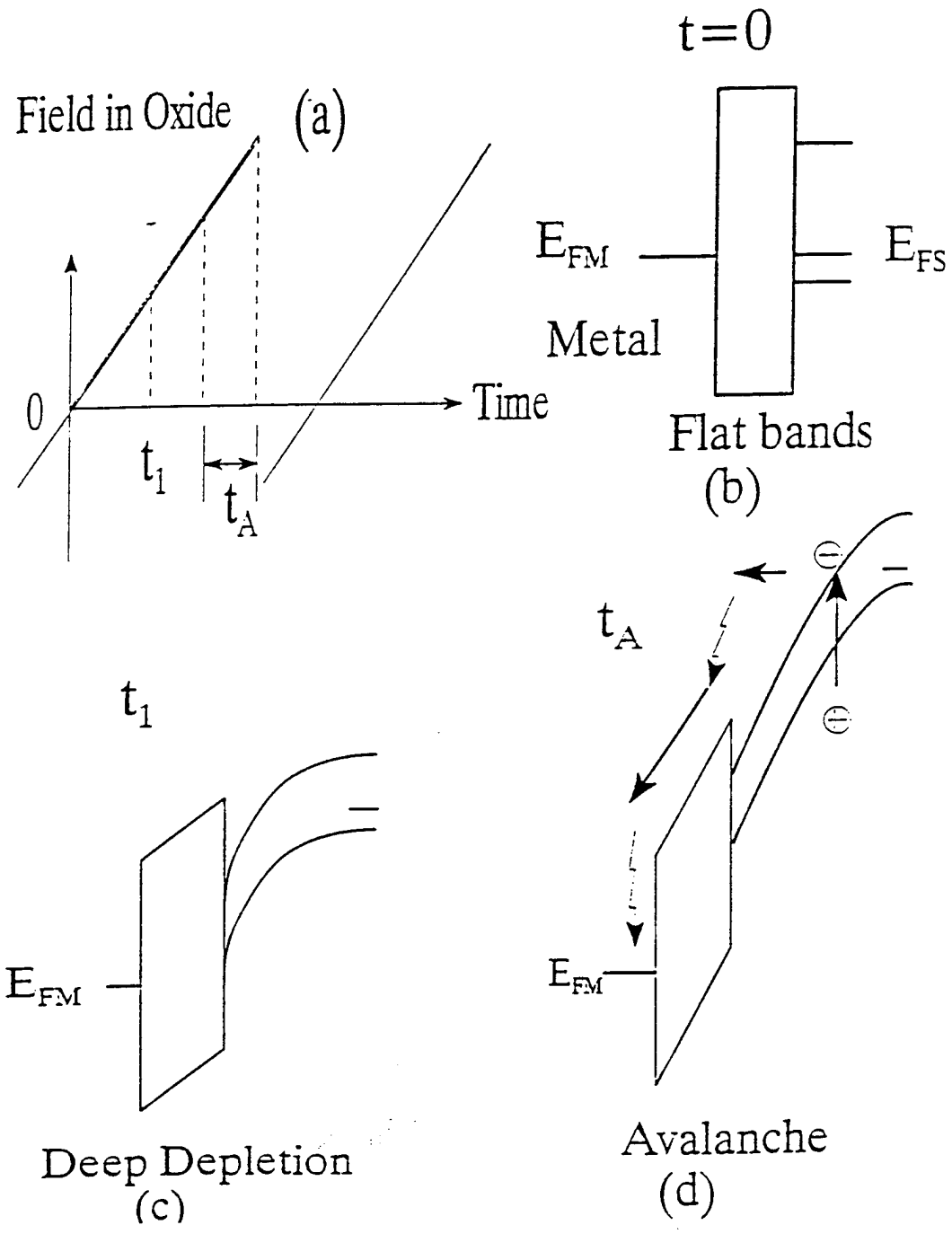


Fig. 3.10 Diagram illustrating the principles of avalanche injection: (a) one cycle of the oxide field is produced by the external ac drive; (b),(c), and (d) show band bending in the silicon at various times during the ac cycle.

During the avalanche interval t_A, electrons are excited from the valence band to the conduction band of silicon by impact ionization. These electrons drift toward the Si-SiO_2 interface under the influence of the electric field in the depletion layer. Most electrons arriving at the interface have energy below the interface barrier height E_b, and these form an inversion layer. However, a few electrons have energy above E_b. Those not scattered back into the silicon at the barrier enter the SiO_2 and drift toward the gate by the electric field across oxide.

The electrons in the inversion layer recombine with holes flowing toward the Si-SiO_2 interface and decrease the field in the silicon depletion layer. The MOS capacitor is then driven into the accumulation condition. During this part of the cycle, holes in the p-type silicon substrate accumulate at the Si-SiO_2 interface. In this falling or accumulation portion of the cycle no electrons are injected. The electrons present are eliminated by recombination with the holes. This portion is definitely needed to eliminate electrons created during the rising avalanche portion of the cycle because these electrons would reduce the depletion layer which is the main source of the avalanche injection. If the inversion layer charge is not completely recombined on one cycle, a higher AC voltage will be required to initiate avalanche on the next cycle.

In avalanche injection, a pulse of electrons is injected into the oxide once per cycle during the rising interval. The instantaneous electron current density at any point during injection is given by[89]:

$$J_n = J_t \exp\left(-\frac{qV_b}{kT_n}\right)\exp\left[\frac{q}{kT_n}\sqrt{\frac{q(V-V_{AV})}{4\pi\epsilon_i d}}\right]\exp\left(-\frac{x_o}{l}\right) \qquad (3.8)$$

where V_b is the barrier height from the Si conduction band to the SiO_2 conduction band, V is the applied voltage, V_{AV} is the silicon avalanche voltage($\sim$10v), ϵ_i is the high-frequency dielectric constant of SiO_2, d is the oxide thickness, k is Boltzmann's constant, T_n is the effective temperature of hot electrons, x_o is the distance to the potential maximum, and l is the electron scattering length in SiO_2. The integral is from the time t_1, at which the avalanche process occurs in the silicon to the time t_2, at which the avalanche period ends in one cycle. J_i in equation 3.8 can be written as

$$J_i = BI_D T_n^2 f \tag{3.9}$$

where B is an arbitrary constant, I_D is the displacement current through the oxide after the onset of avalanche, and f is the frequency of the applied AC voltage. In the above two expressions, we can see that the avalanche current density is a function of amplitude and frequency of the applied AC voltage.

3.3.2 Experimental Set-up

The experimental set-up of the avalanche injection system designed by D.R.Young[88] is shown in figure 3.11. During the whole process of avalanche charge injection, the average DC current is kept at a constant value. A 150 KHz sawtooth signal is generated by an HP 3310A function generator as the applied voltage source for avalanche injection. The automatic data acquisition system is available to monitor the flatband voltage as a function of time or charge fluence.

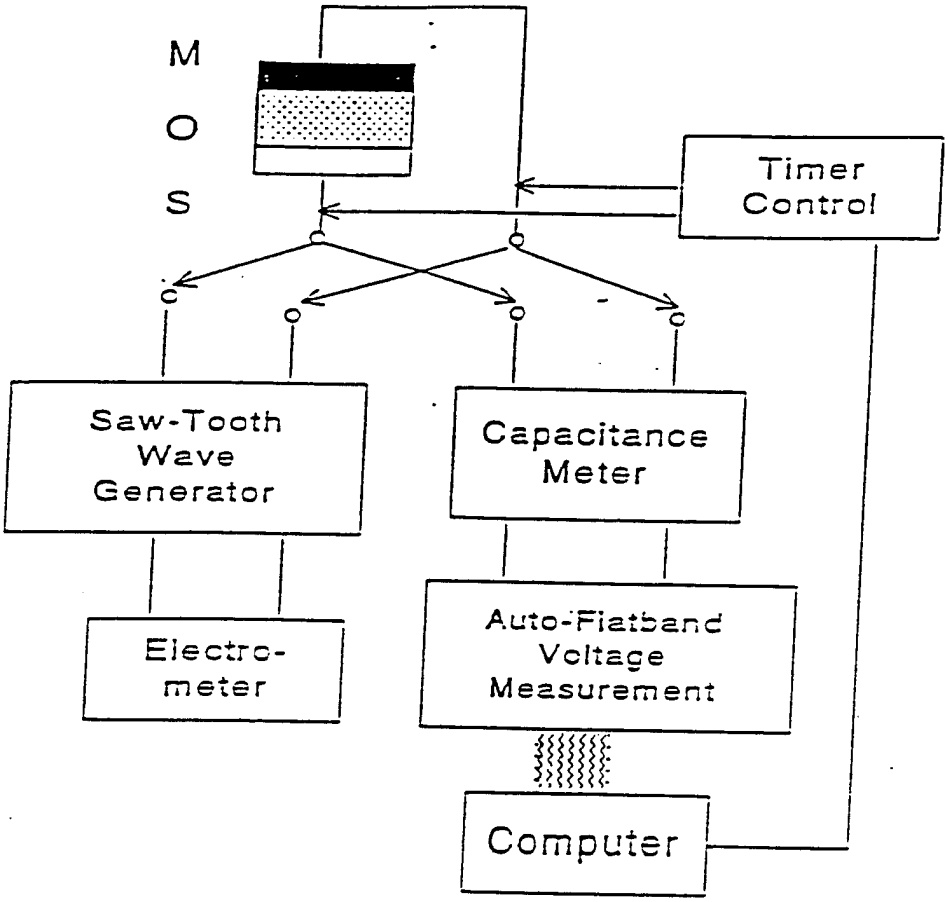


Fig. 3.11 Experimental set-up of the Avalanche Injection.

3.3.3 Hot Electron Study by Avalanche Injection

To study the hot electron injection of MOS, the injection current must be emission limited. That is, it is essential that trapping in the oxide be negligible. The varied injection current and the corresponding voltages are carefully monitored. A typical current vs. voltage curve is shown in figure 3.12.

The electron energy distribution can be calculated from the current vs. voltage

curve. Figure 3.13 shows the energy band diagram in SiO_2 during avalanche injection. In this case we assume that the current that flows through the oxide is equal to that portion of the electron distribution with energies in excess of barrier energy. So the injection current is

$$J=\frac{q}{T}\int_{\phi_B}^{\infty} N(\phi_B)d\phi_B \tag{3.10}$$

where ϕ_B is the Si-SiO_2 barrier height, q is electron charge and T is injection period.

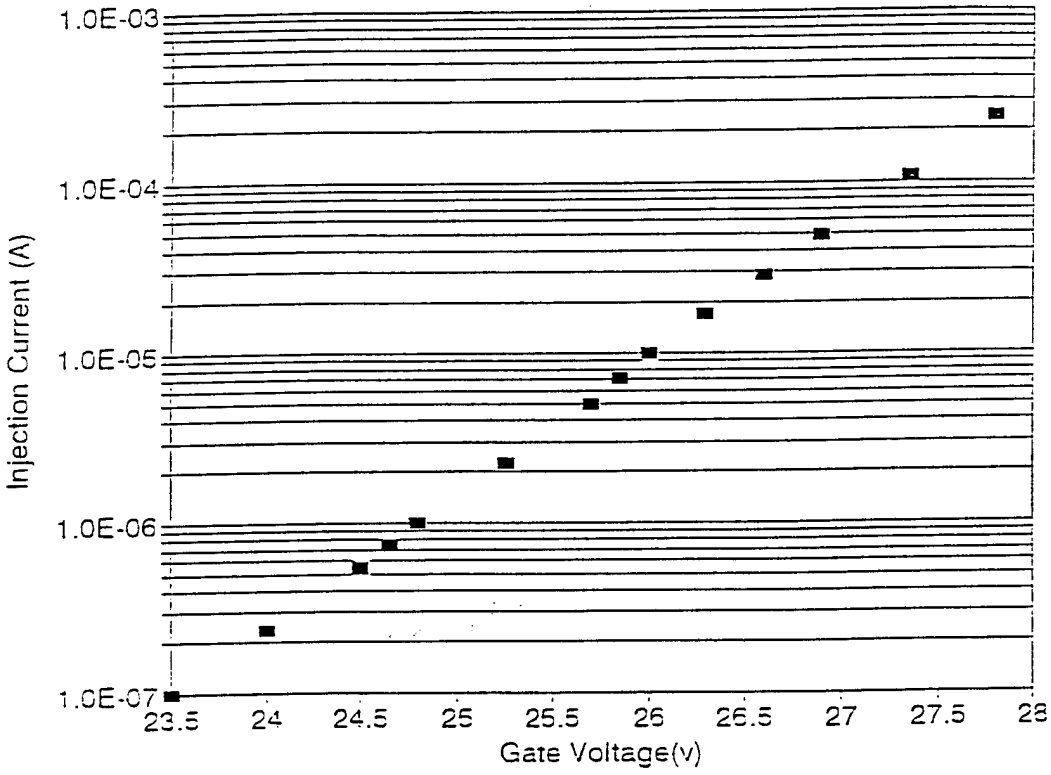


Fig. 3.12 Avalanche Injection current versus Gate voltage.

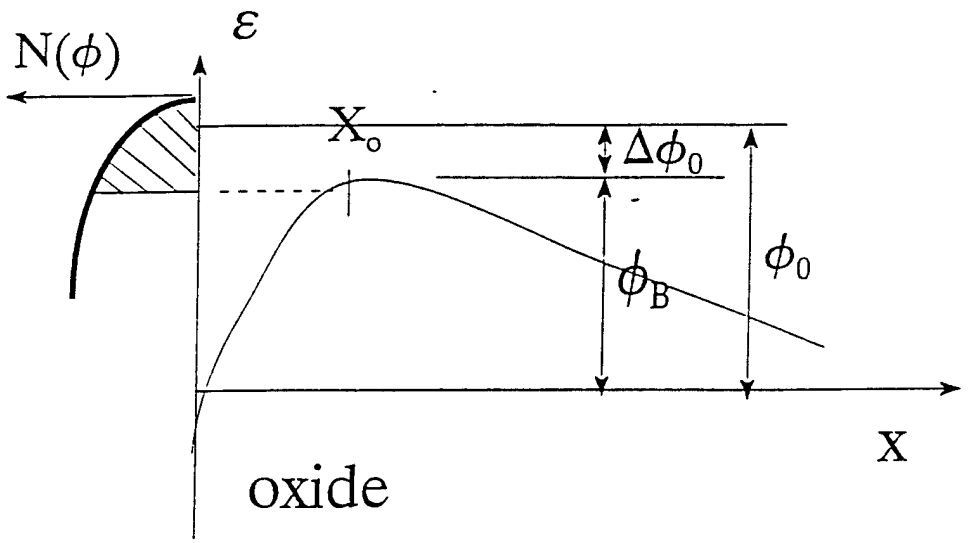


Fig. 3.13 Energy band diagram in SiO_2 during Avalanche Injection.

The relationship between ϕ_B and the oxide field is given by[90]

$$\phi_B=\phi_o-\Delta\phi_o \tag{3.11}$$

where ϕ_o is zero field barrier height of SiO_2 which is 3.1 eV, $\Delta\phi_o$[91] is barrier lowering by E_{ox} which is $(q/4\pi k\epsilon_o E_{ox})^{1/2}$, $\epsilon=8.85\times10^{-14}$, and k=2.15 is the optical dielectric constant of SiO_2. The derivative of Eq. 3.9 with respect to ϕ_B yields.

$$N(\Phi_B)=-\frac{T}{q}\frac{dJ}{d\phi_B} \tag{3.12}$$

The result is plotted in Fig. 3.14.

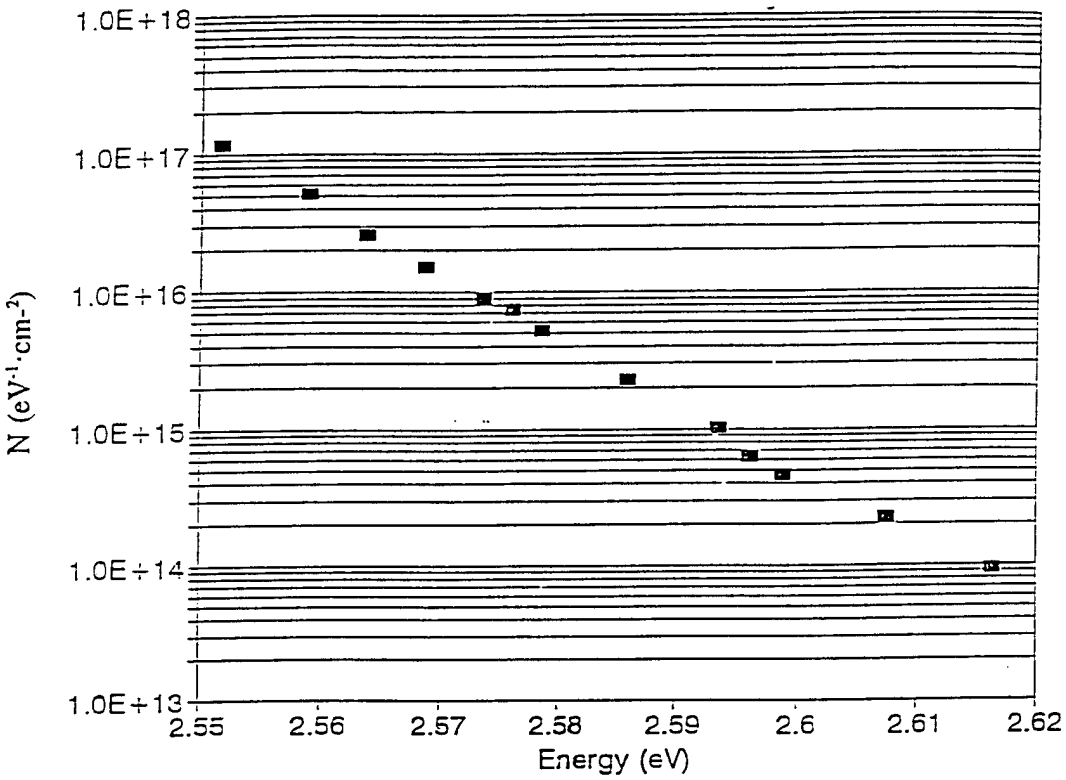


Fig. 3.14 Hot carrier energy distribution curve.

One of the original contributions made in this work is the development of this technique to enable us to calculate the energy distribution of the hot carriers from data taken using MOS capacitors.

3.3.4 Oxide Charge Trapping

Two useful parameters associated with charge trapping property can be extracted from this technique: (1) The trap capture cross section (σ) and (2) The trap density per unit area (N). First, the automatic data acquisition system monitors the flatband voltage shift as a function of time. Figure 3.15 is a typical curve of the avalanche charge injection.

The analysis of the data is based on fitting exponential curves to the results. The relationships between the voltage shift ΔV and time t for a single trap can be written as

$$\Delta V=\Delta V_f[1-\exp(-\frac{t}{\tau})] \tag{3.13}$$

where ΔV_f is the voltage change if the measured single trap is filled and τ is the time constant related to the trap cross section as follows

$$\sigma=\frac{q}{\tau J} \tag{3.14}$$

where q is the electron charge and J is the average DC current density. The trap density per unit area, N_T, is given by

$$N_T = \frac{\epsilon_o}{q x_i} \Delta V \tag{3.15}$$

where ϵ_o is the low frequency dielectric constant of SiO_2 and x_i is the distance to the charge centroid as measured from the metal electrode.

If more than one trap is involved in the measured curves, it is necessary to use the summation of all these different traps, therefore

$$\Delta V = \sum_i \Delta V_{fi} [1 - \exp(-\frac{t}{\tau_i}) \tag{3.16}$$

To fit these exponentials, one needs to calculate the derivative, $d\Delta V/dt$, from the experimental data and to extract trap capture cross section, σ_i, and trap density, N_{Ti}, via a plot of $\ln(d\Delta V/dt)$ versus t[92].

The range of silicon doping density is crucial for uniform charge injection. Previous work has shown that avalanche injection is useful only over a limited range of silicon doping density (5×10^{16} -10^{18} cm^{-3})[93]. Beyond the upper limit, interband tunneling rather than avalanche breakdown occurs in the silicon. Below the lower limit, the edge avalanche breakdown occurs before avalanche breakdown occurs in the center of the MOS capacitor. Therefore, the depletion layer width can not be driven to its maximum value and uniform injection is not guaranteed. Another problem of low doping density sample is the breakdown of the oxide during the accumulation portion of the AC cycle. This is not a problem for the waveforms we use since the voltage applied during accumulation is small. As doping density is decreased, avalanche breakdown voltage

increases. At voltages sufficiently high to cause avalanche, the dielectric breakdown strength of the oxide would be exceeded during the accumulation portion of the cycle. Based on the above discussion, the silicon doping densities of the samples in this work were chosen in the range of 6×10^{16} - 2×10^{17} cm^{-3} to assure uniform injection.

3.4 I-V Measurement for MOSFET

3.4.1 Introduction

The Ge doped MOSFET characterization for the extraction of carrier mobility was carried out using a a four point thermal probe station which allowed for microscopic inspection and probing of the MOSFET. The probe station was connected to a Hewlett-Packard 4145B semiconductor parameter analyzer with an assorted Hewlett-Packard 7475 plotter.

By fixingg the drain to source voltage V_{DS} and conducting a gate voltage V_{GS} sweep for each value of the drain voltage we can generate different I_D-V_{GS} curves. We can thus derive the field-effect mobility for the MOSFET.

3.4.2 Mobility Extraction

When a n-channel MOSFET is biased at moderate drain voltage, the drain current is given as a function of drain voltage V_{DS} and gate voltage V_{GS}[94].

$$I_{DS}=\frac{Z\overline{\mu}_n C_{ox}}{L}\{[V_{GS}-V_T-\frac{V_{DS}}{2}]-\gamma[\frac{2}{3}(V_{DS}+2\phi_F')^{\frac{3}{2}}-\frac{2}{3}(2\phi_F')^{\frac{3}{2}}-V_{DS}(2\phi_F')^{\frac{1}{2}}]\} \quad (3.17)$$

where $\bar{u}_n$ is the MOSFET mobility and V_T is the *threshold voltage*, which is defined as

$$V_T = V_{FB} + 2\phi_F + \gamma(2\phi_F')^{\frac{1}{2}} \tag{3.18}$$

where V_{FB} is the flatband voltage, ϕ_F' is the Fermi potential and γ is the body factor. The definitions of these parameters are described in the reference.

The field effect mobility can be derived from eq. 3.18. Taking the derivative with respect to the gate voltage, equation (3.17) yields

$$\left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=constant} = \frac{Z\overline{\mu}_n C_{ox}}{L} V_{DS} \tag{3.19}$$

where $\partial I_D/\partial V_{GS}$ is the transconductance g_m. eq.(3.19) can be solved for the field-effect mobility (μ_{FE}) as

$$\mu_{FE} = \frac{Lg_m}{ZC_{ox}V_{DS}} \tag{3.20}$$

3.5 Device Process Procedure

3.5.1 MOS Capacitor Process

Figure 3.15 shows the process procedure for the germanium implanted MOS capacitor. p-type, <100>, silicon wafers are used. Thermally dry oxides were grown

on silicon substrates at 1000°C for 45 minutes in a double wall furnace after RCA cleaning. The oxide thickness is about 450 Å. An nitrogen ambient post-oxidation anneal (POA) is performed right after oxidation for 20 minutes at the same temperature. Then germanium is implanted into the Si-SiO_2 interface. The implantation is performed by *KROKO* in California. The energy used is around 75 KeV, the dose ranges from 10^{12} /cm^2 to 10^{15} /cm^2. After implantation, the wafers are annealed at 950°C for 30 minutes. A layer of aluminum is deposited on the top by an evaporator. Photolithography is performed to defined the gate with an area of 0.01 cm^2. At last, all samples are subjected to post metallization annealing (PMA) at 450°C in forming gas (20% H_2 +80% N_2) for 30 minutes.

3.5.2 MOSFET Process

N-channel MOSFET's are fabricated with and without Ge doping. The starting material is a p-type, <100>, 2-3 Ω-cm 3-inch wafer. The MOSFET's have a gate oxide thickness of 400 Å. The channel length is 10 μm long and 50 μm wide. Ge is implanted throughout the channel region before the gate oxidation growth with energy of 30 KeV and dose of 10^{14}/cm^2. The detail of the fabrication process of MOS capacitor and MOSFET are described in the Appendix A and B.

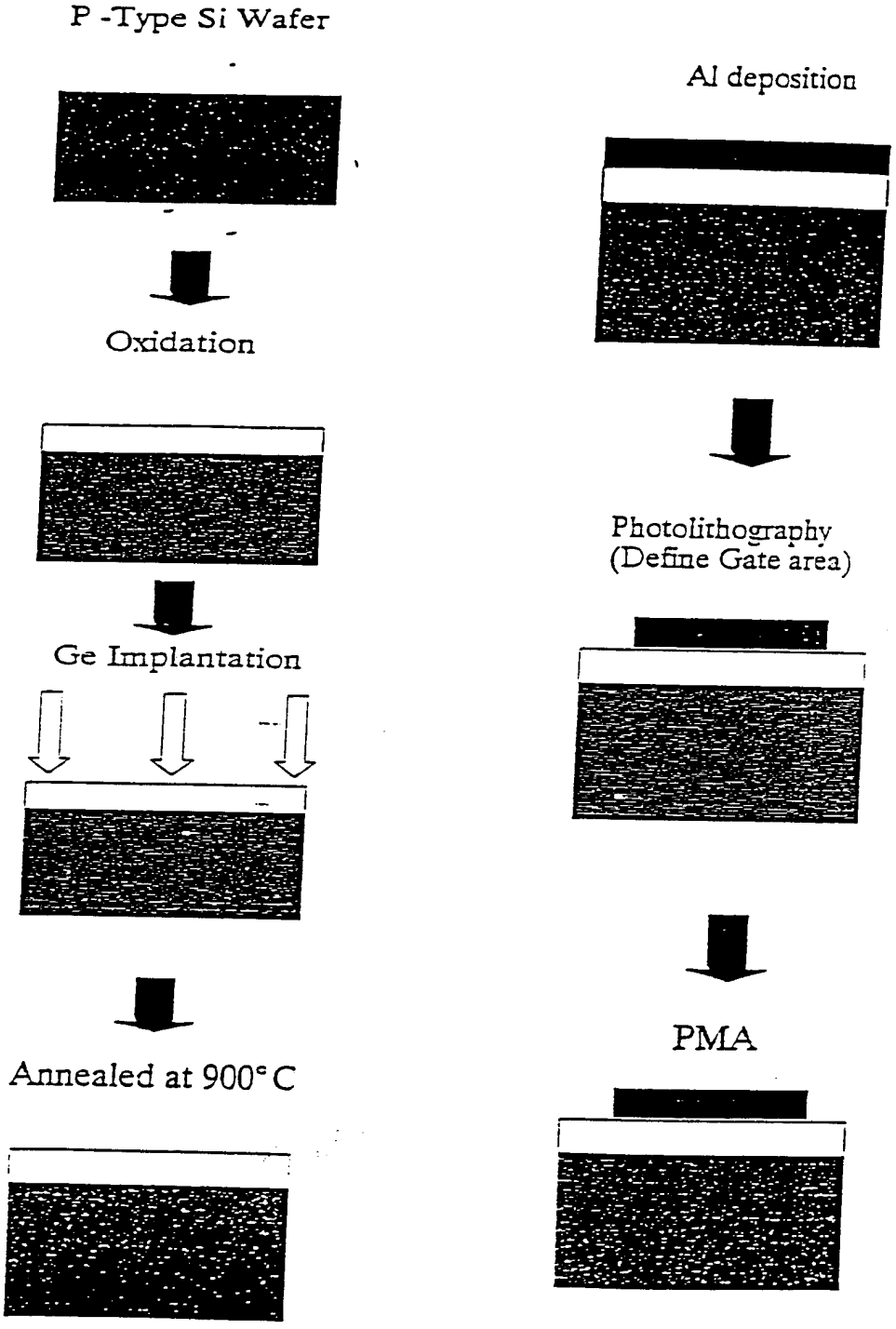


Fig. 3.15 Ge implanted MOS capacitor process procedure.

Chapter 4
Results and Discussion

4.1 Introduction

In this chapter, the experimental results measured by the techniques described in chapter three will be presented. To determine the optimum Ge implantation conditions, a systematic study of the effect of the variation of the implantation dose and energy was conducted. First, the electrical properties of the MOS capacitor implanted with different doses of Ge are examined and a optimum dose determined. To study the effect of the peak position of the germanium concentration profile, different implantation energies have been used. The effect of the implantation energy on the electrical properties will be presented. To reduce the density of the traps in the oxide, a modified process has been proposed. The comparisons between the samples made by the modified process and the original process have been made. The hot carrier injection of the Ge implanted sample at liquid nitrogen temperature has also been measured and a large reduction was observed. Germanium implanted n-channel MOSFET's were manufactured to investigate the channel carrier mobility. As a comparison with germanium, we have implanted carbon into the MOS capacitors. These carbon implanted samples have also been evaluated. The comparison between C and Ge implanted samples will be presented in the last section.

4.2 Properties of Ge Implanted Sample

4.2.1 C-V Characterization

A high frequency charge voltage measurement was performed to evaluate the interface characteristic of the germanium implanted samples. The results are shown in figure 4-1(a)-(d). In figure 4-1(a) and (b), The C-V curves of germanium implanted sample are very close to the curves of their control samples. In fig 4-1(c), we see stretch-out in the Ge implanted sample for a dose of $10^{14}/cm^2$, the stretch increase in fig 4-1(d) for a dose of $10^{15}/cm^2$.

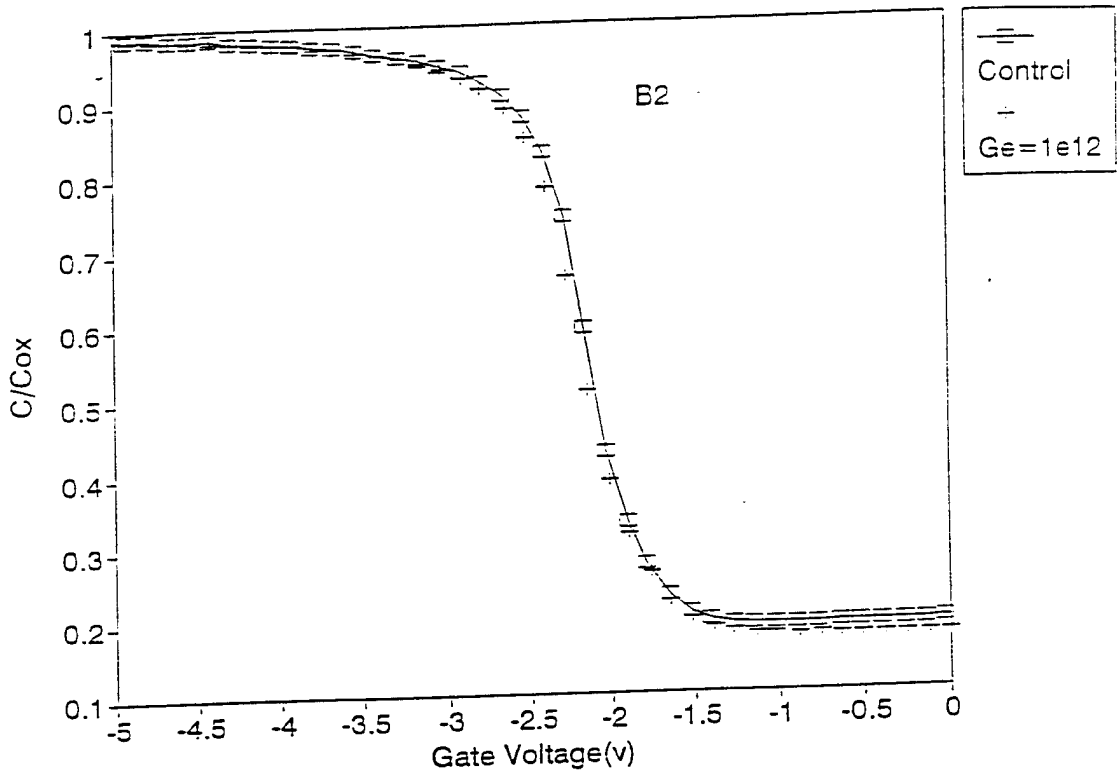


Fig. 4.1(a) The high frequency C-V curves for Ge implanted (Dose=$10^{12}/cm^2$, energy=70 Kev) MOS and the control sample. The "+" is the Ge implanted sample, "□" is the control sample.

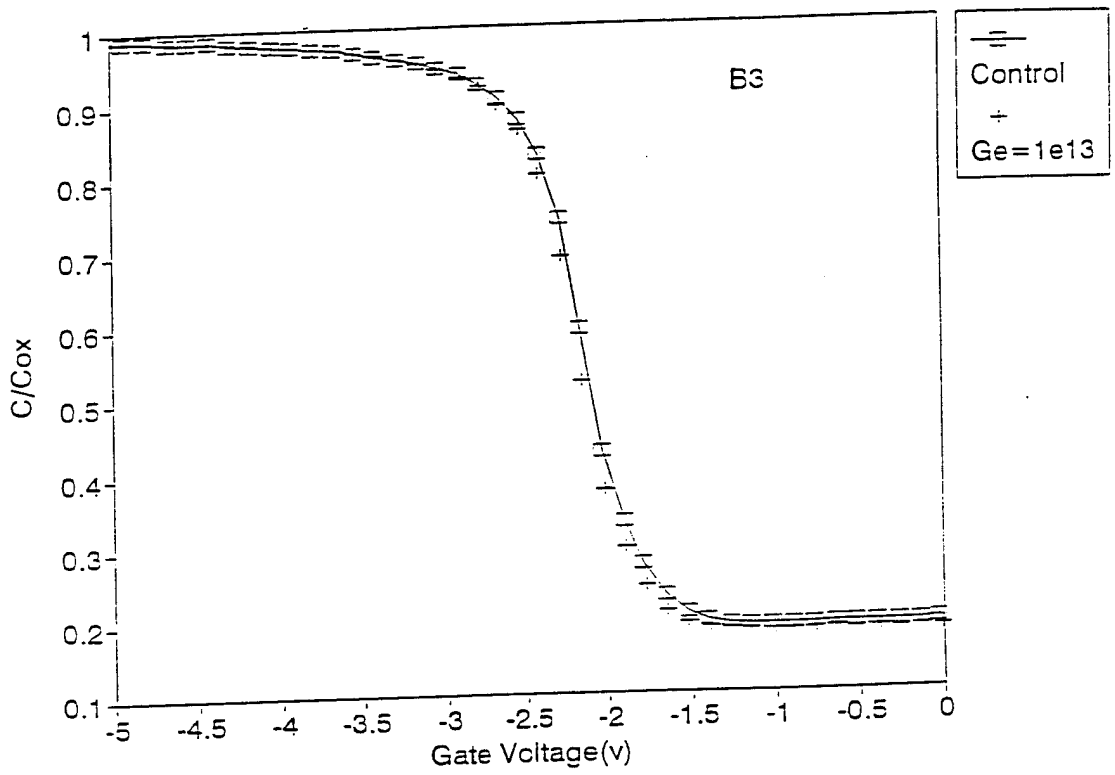


Fig. 4.1(b) The high frequency C-V curves for Ge implanted (Dose=10^{13}/cm^2, energy=70Kev) MOS and the control sample. The "+" is the Ge implanted sample, "□" is the control sample.

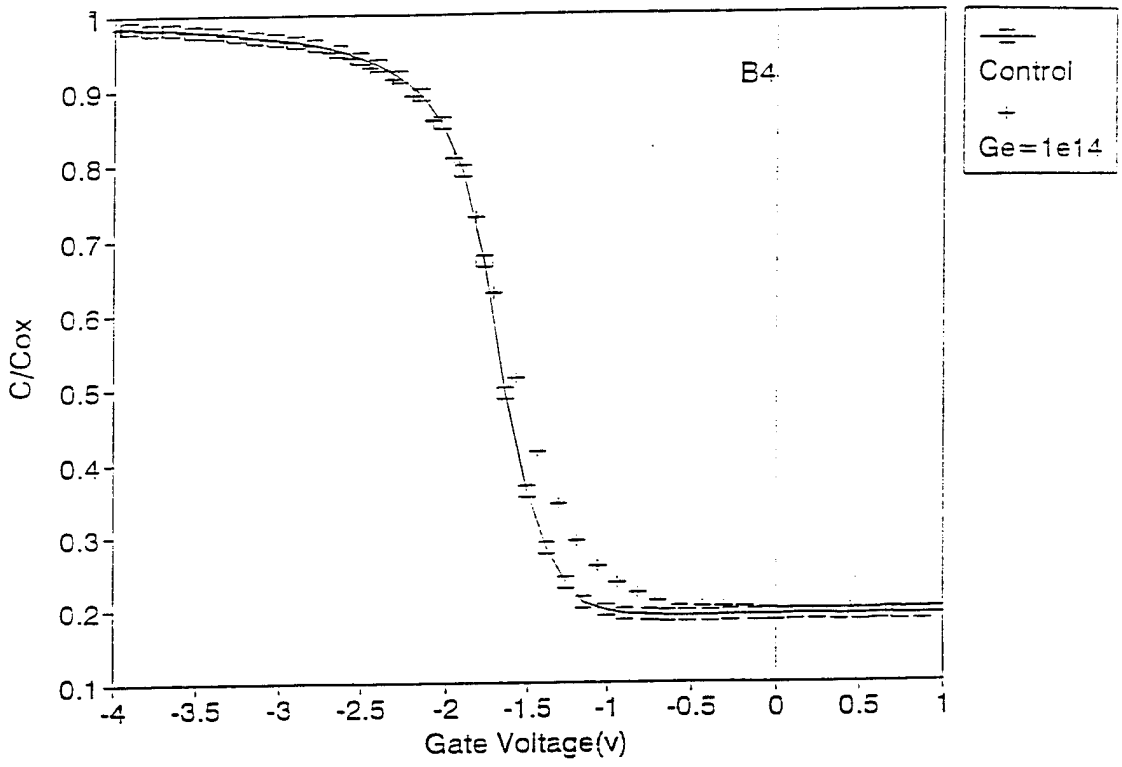


Fig. 4.1(c) The high frequency C-V curves for Ge implanted (Dose=10^{14}/cm^2, energy=70 Kev) MOS and the control sample. The "+" is the Ge implanted sample, "□" is the control sample.

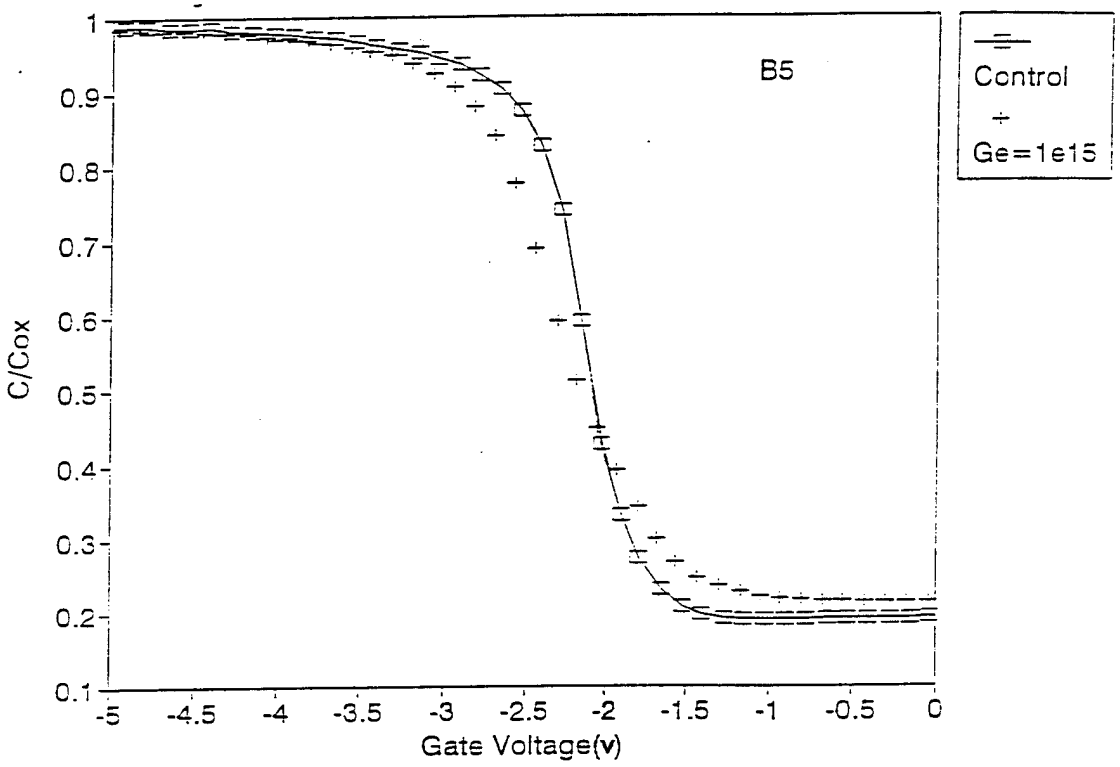


Fig. 4.1(d) The high frequency C-V curves for Ge implanted (Dose=10^{15}/cm^2, energy=70 Kev) MOS and the control sample. The "+" is the Ge implanted sample, "□" is the control sample.

The results of C-V measurement show that Ge implantation does not change charge characteristic of MOS if the Ge dose is lower than 10^{14} /cm^2. If the germanium dose is greater than 10^{14} /cm^2 the interface state density is increased. There is no parallel shift in all cases which indicates the introduction of germanium does not change the fixed charge of the MOS.

4.2.2 Q-V Measurement Results

Charge-voltage (Q-V) characterization was performed for the germanium implanted MOS capacitors. The surface potential as a function of gate voltage curves for all samples is shown in figure 4.2(a)-(d). We discover a stretch-out in ψ_s-V curve when the dose of Ge is larger than 10^{14} /cm^2. This stretch-out is caused by the interface state density increase which also results in the C-V curve stretch-out that was discussed in the last section. According to reference 63, the presence of germanium in Si can decrease the bandgap in the silicon, because the Ge has smaller bandgap than Si. In our ψ_s-V curves, there is no change in the bandgap, because the largest Ge mole concentration in our study is only 0.5 % which is not sufficient to introduce noticeable bandgap reduction according to fig. 2.8.

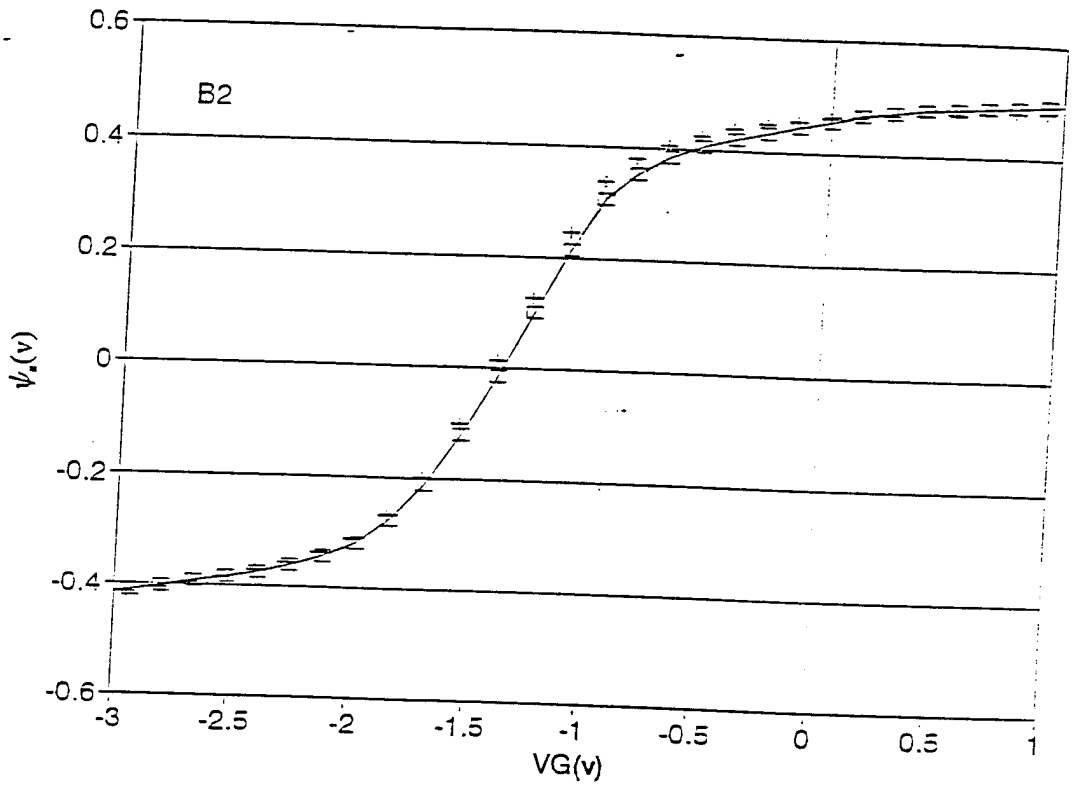


Fig. 4.2(a) Surface potential versus Gate voltage curves for $10^{12}/cm^2$ Ge implanted MOS and control sample. The "+" is the Ge implanted sample, the "□" is the control sample.

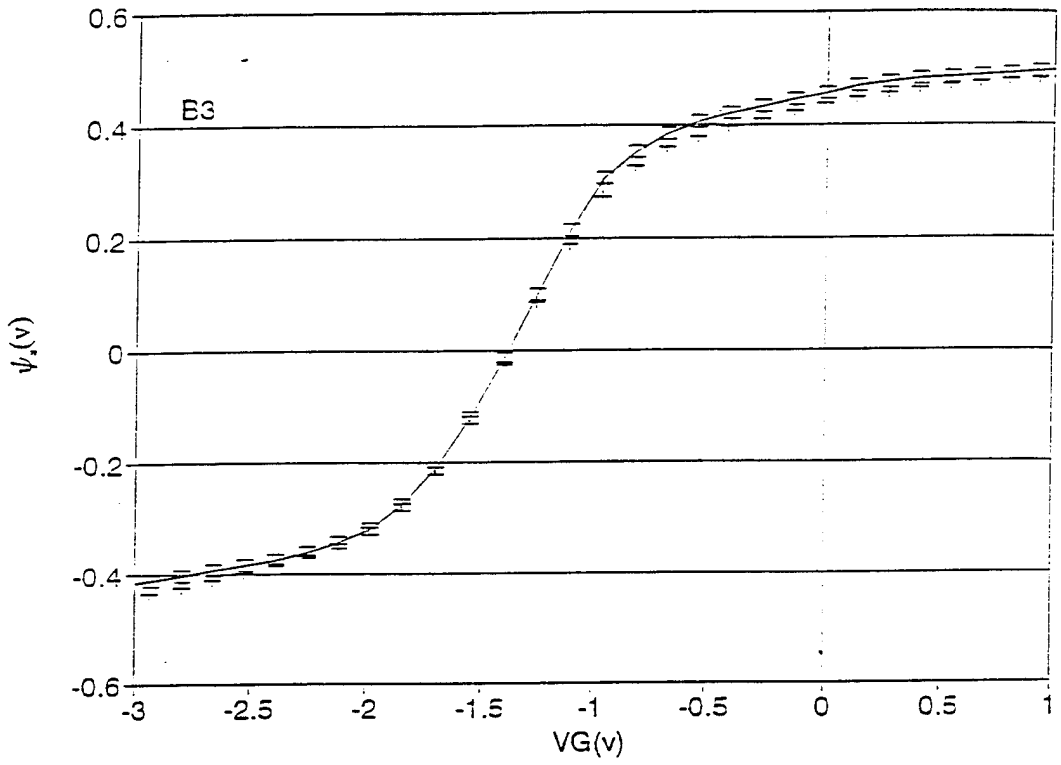


Fig. 4.2(b) Surface potential versus Gate voltage curves for $10^{13}/cm^2$ Ge implanted MOS and control sample. The "+" is the Ge implanted sample, the "□" is the control sample.

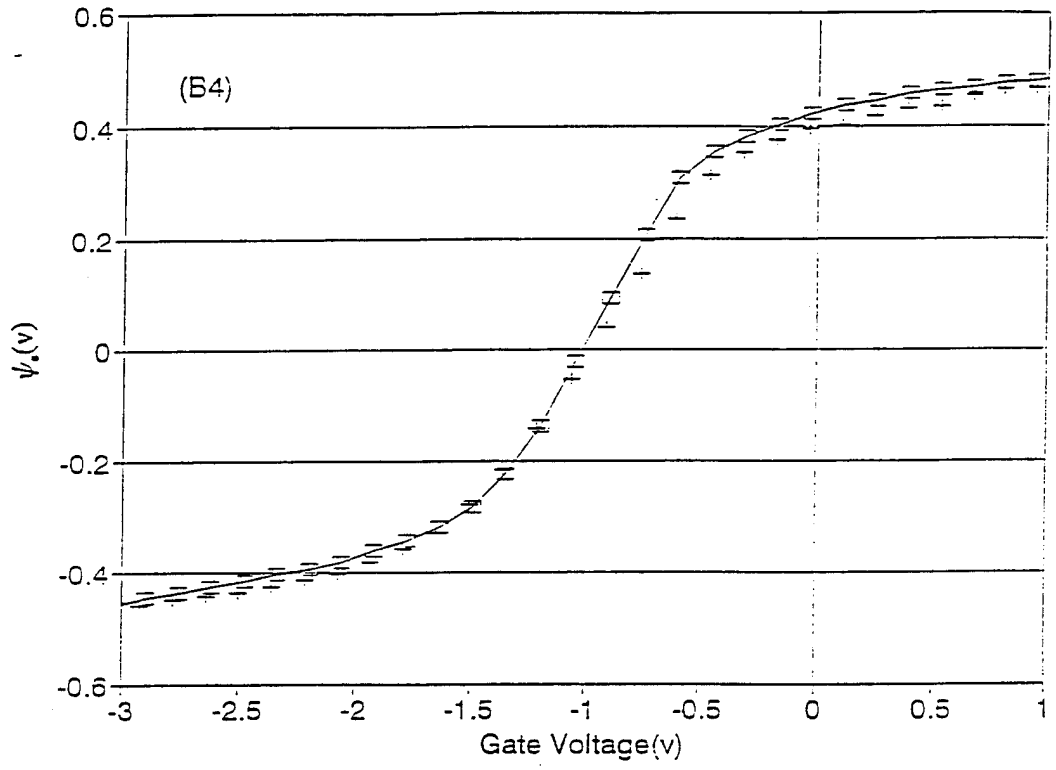


Fig. 4.2(c) Surface potential versus Gate voltage curves for $10^{14}/cm^2$ Ge implanted MOS and control samples. The "+" is the Ge implanted sample, the "□" is the control sample.

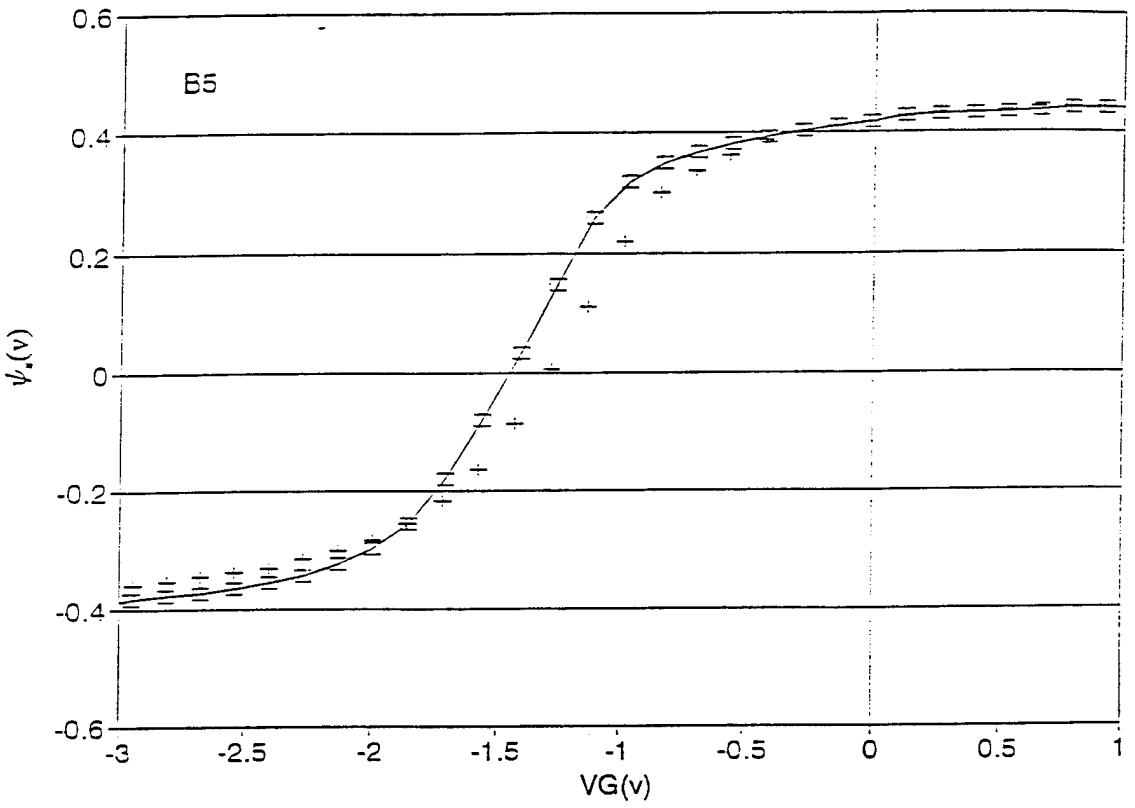


Fig. 4.2(d) Surface potential versus Gate voltage curves for $10^{15}/cm^2$ Ge implanted MOS and control sample. The "+" is the Ge implanted sample, the "□" is the control sample.

By using the surface potential versus gate voltage data, the interface trap densities were obtained using the method described in chapter three. From figures 4.3(a)-(c), the increase with interface state densities can be clearly seen in the case of a Ge dose greater than $10^{14}/cm^2$. The interface state density at midgap against Ge dose curve is plotted in fig 4.4. From this curve, we can clearly see how the interface state density changes with the Ge dose.

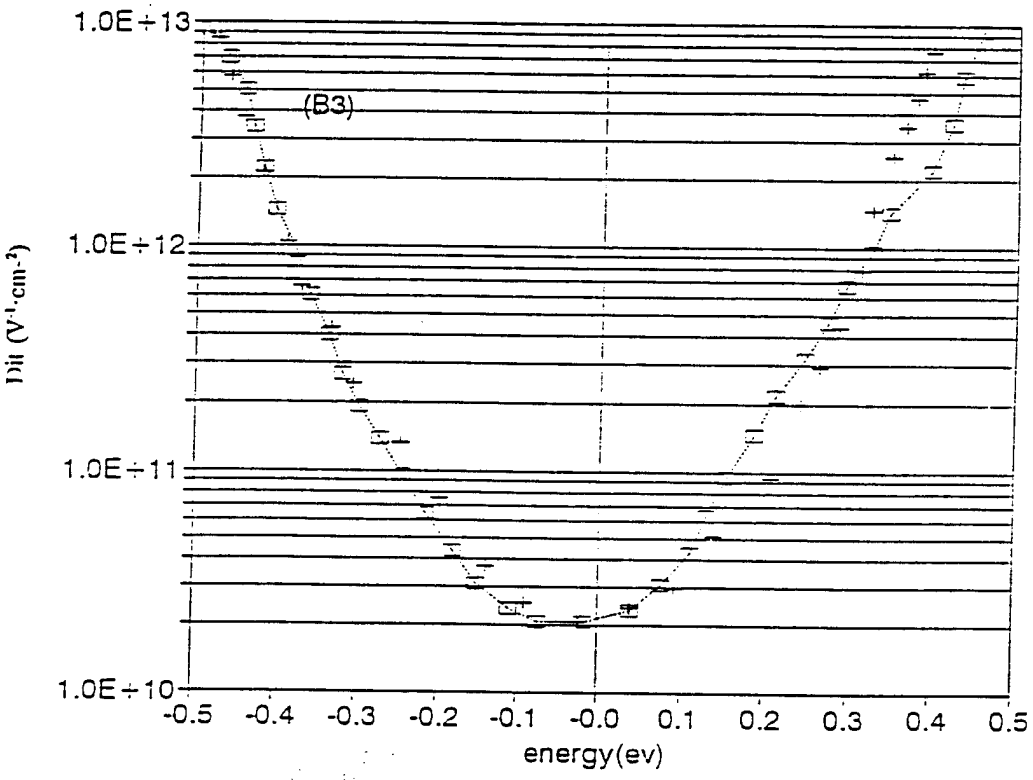


Fig. 4.3(a) Interface state density versus energy curves for Ge implanted (dose < $10^{13}/cm^2$) and control samples. The "+" is the Ge implanted sample, the "□" is the control sample.

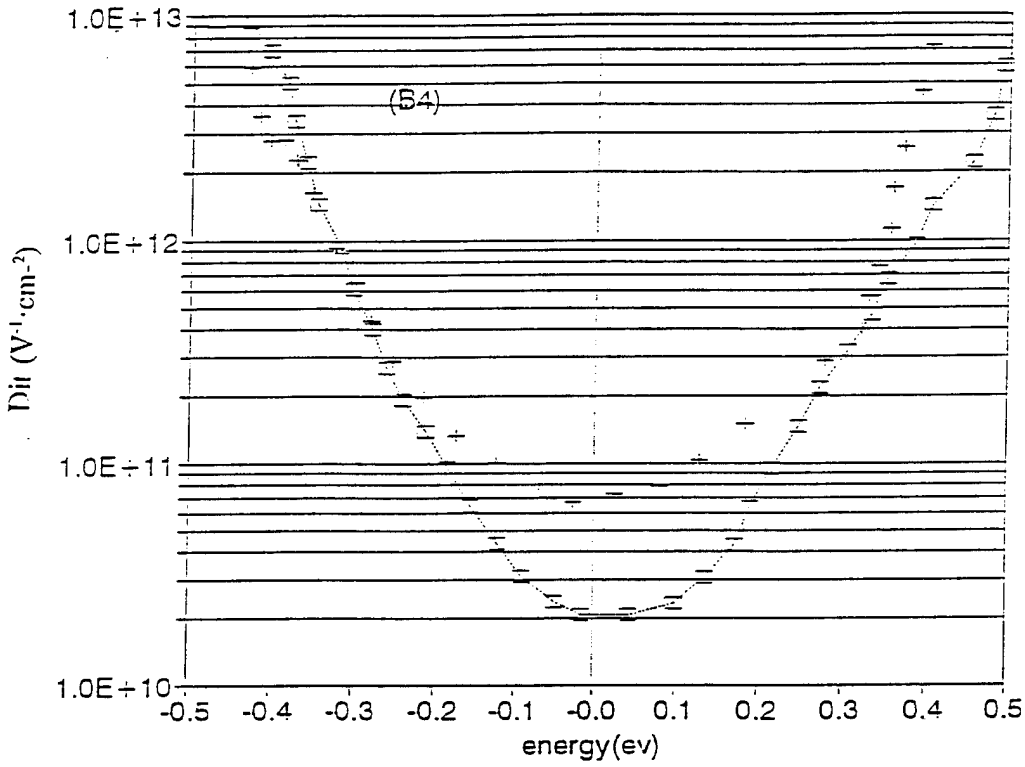


Fig. 4.3(b) Interface state density versus energy curves for Ge implanted (dose= $10^{14}/cm^2$) and control samples. The "+" is the Ge implanted sample, the "□" is the control sample.

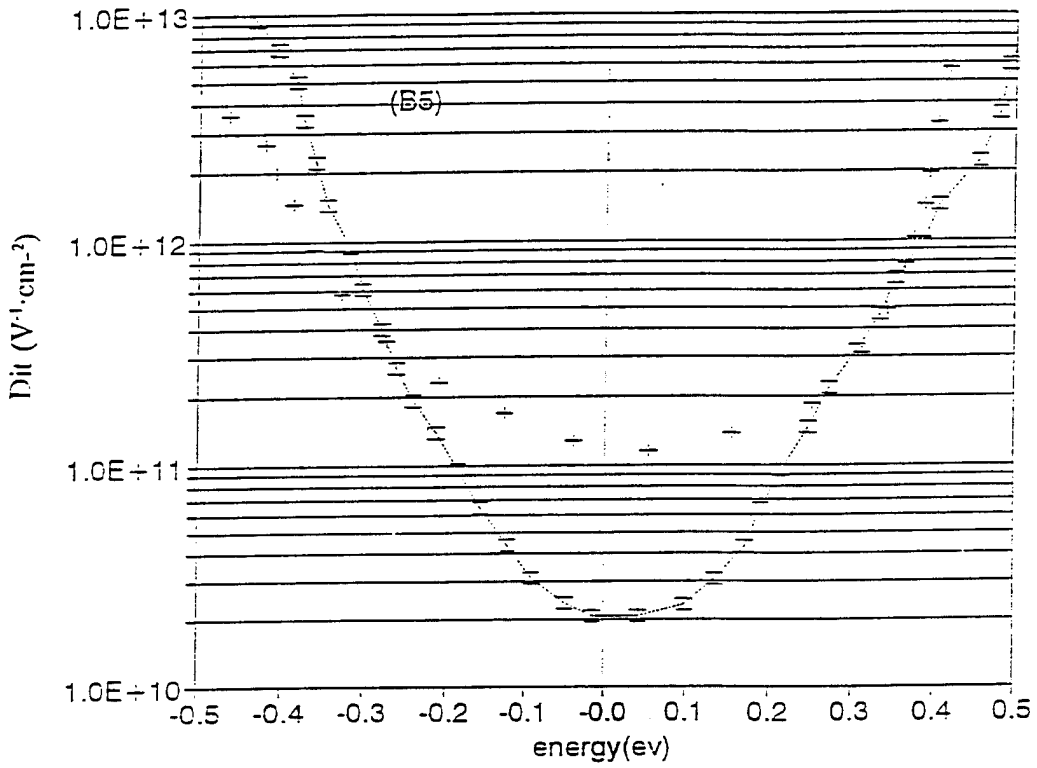


Fig. 4.3(c) Interface state density versus energy curves for Ge implanted (dose= $10^{15}/cm^2$) and control samples. The "+" is the Ge implanted sample, the "□" is the control sample.

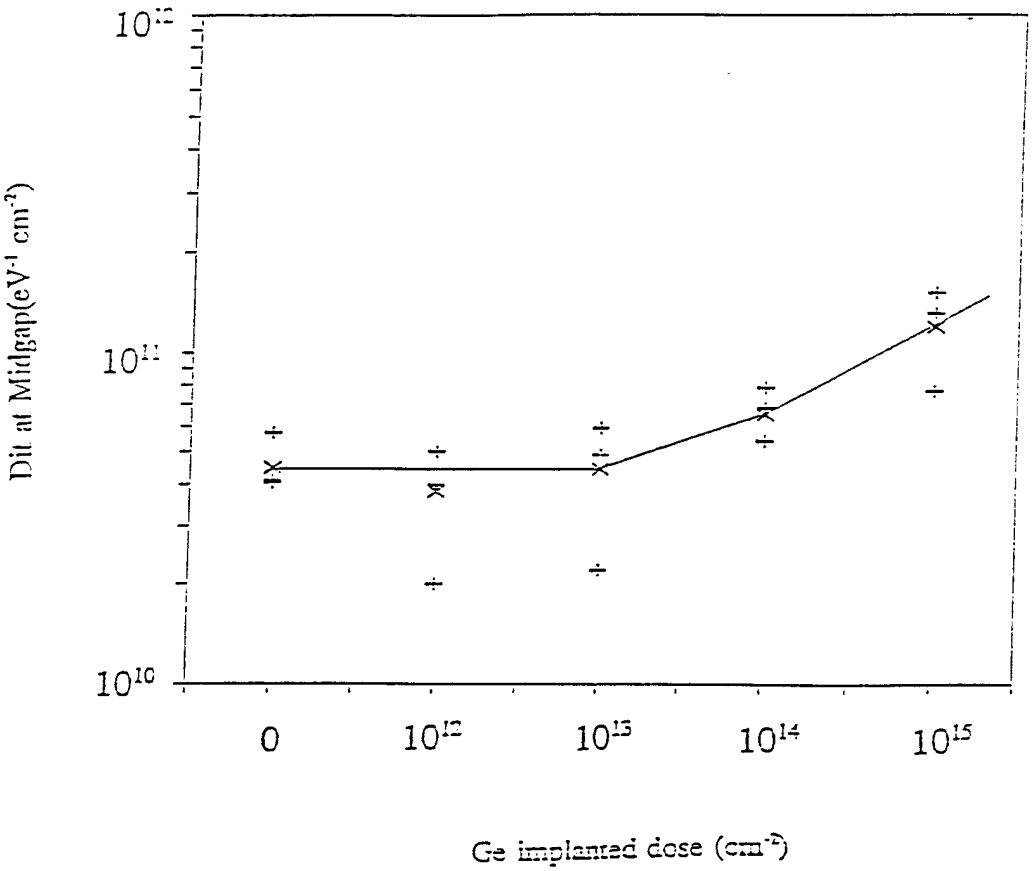


Fig. 4.4 Interface state density at midgap versus Ge dose. For each dose, "+"s are measured Dit, "x" is the average Dit.

4.2.3 Hot carrier Study by Avalanche Injection

The avalanche injection technique was preformed to generate the hot carrier injection for all samples. Figure 4.5 shows the injection current as a function of gate voltage results. All the germanium implanted samples have lower injection current than that of the control sample and the amount of reduction is proportion to the Ge dose. This results clearly shows that the present Ge reduces the hot carrier population in the silicon during hot carrier injection.

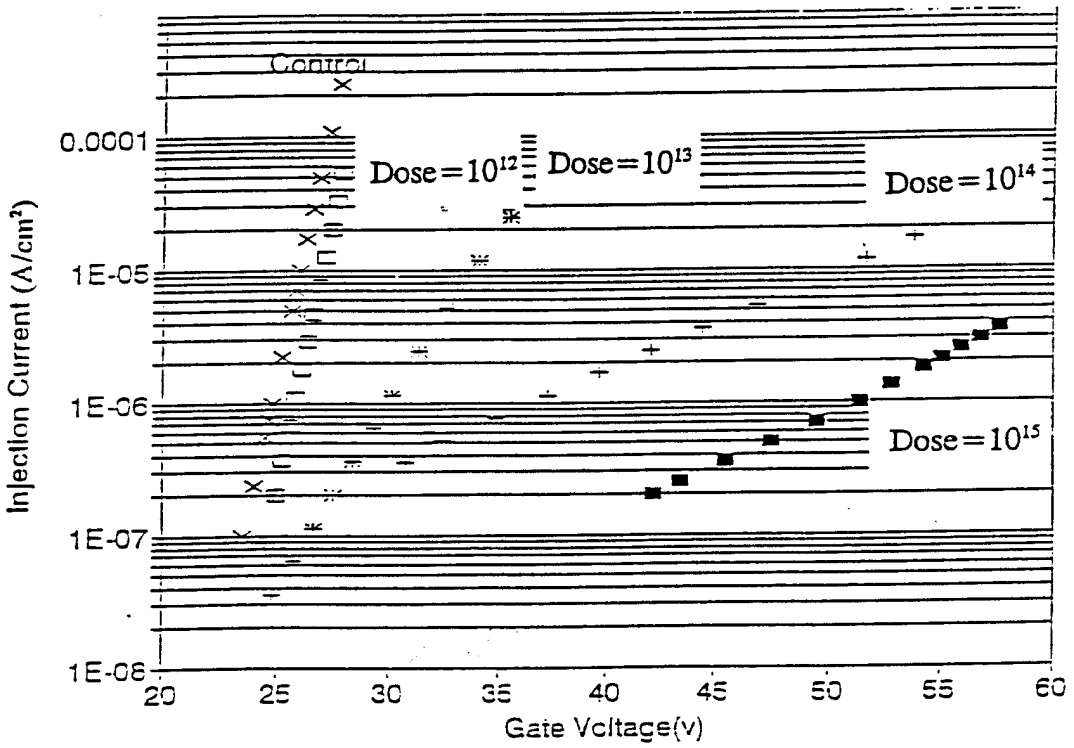


Fig. 4.5 Injection current versus Gate voltage curves for Ge implanted samples.

The hot carrier energy distribution curves were calculated by the method described in chapter three and plotted in figure 4.6. Note the hot carrier distribution has the Maxwelliam form for all samples. The energy of the hot carriers is strongly reduced with the increase of germanium concentration. We also notice the slope of the curve is reduced. This can be explained by the introduction of an additional scattering mechanism that makes hot carrier distribution broader.

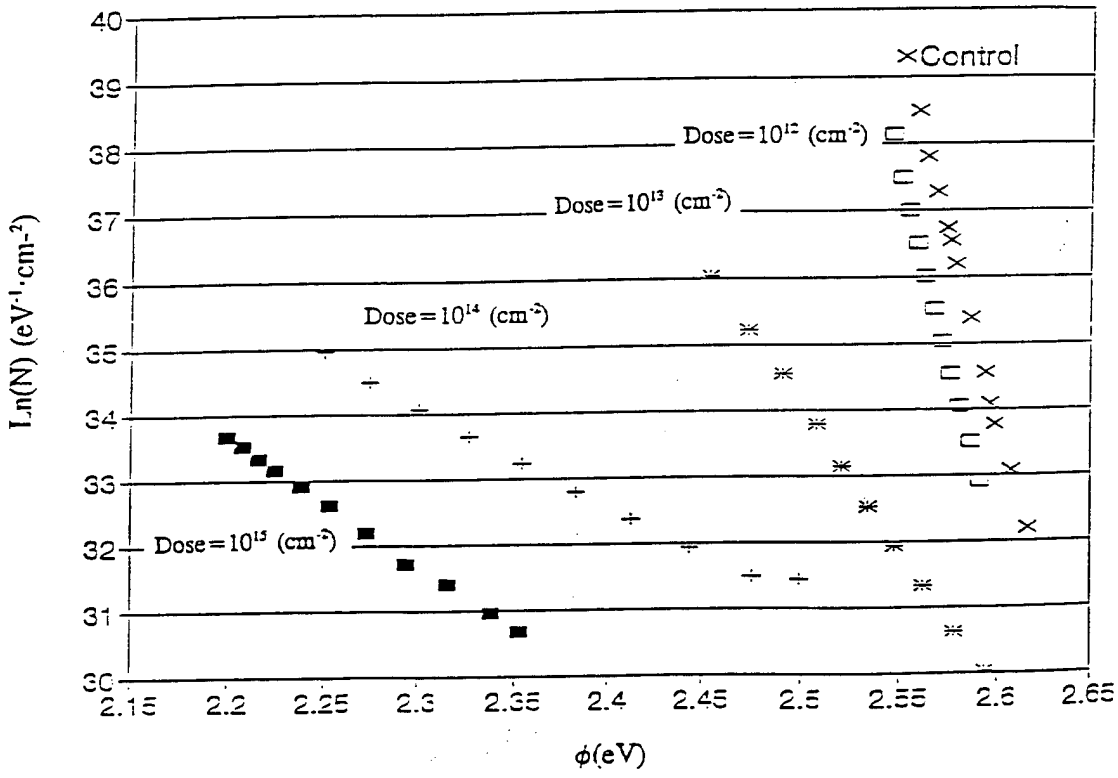


Fig. 4.6 Hot carrier energy distribution curves calculated from figure 4.5.

4.2.4 Carrier Mobility in Ge Implanted MOSFET's

In the hot carrier injection experiment described above, the Ge in the silicon can reduce the hot carrier injection current because an addition scattering mechanism is introduced by the Ge. It is important to determine if the additional scattering mechanism will reduce the mobility of the carriers in the MOSFET's channel. The Ge implanted n-channel MOSFET's are fabricated according to the procedure described in chapter 3. The I-V curves of the Ge implanted MOSFET and Control MOSFET are plotted in figure 4.7(a), (b). The effective mobility of the Ge implanted sample is 645 $cm^2/V \cdot sec$ and the mobility of the control sample is 643 $cm^2/V \cdot sec$. This result shows that the scattering mechanism introduced by Ge does not affect the channel carriers appreciably. This is a significant, favorable result for germanium implantation.

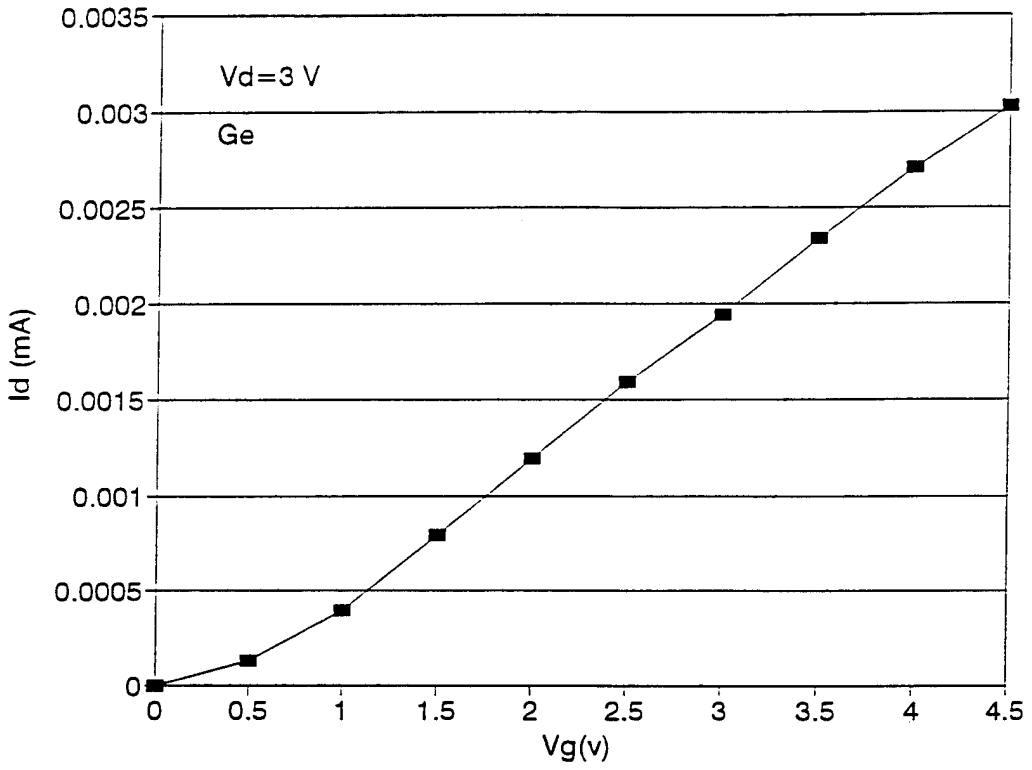


Fig. 4-7(a) I-V curves of Ge implanted n-channel MOSFET. The channel length is 10μm, oxide thickness is 370Å.

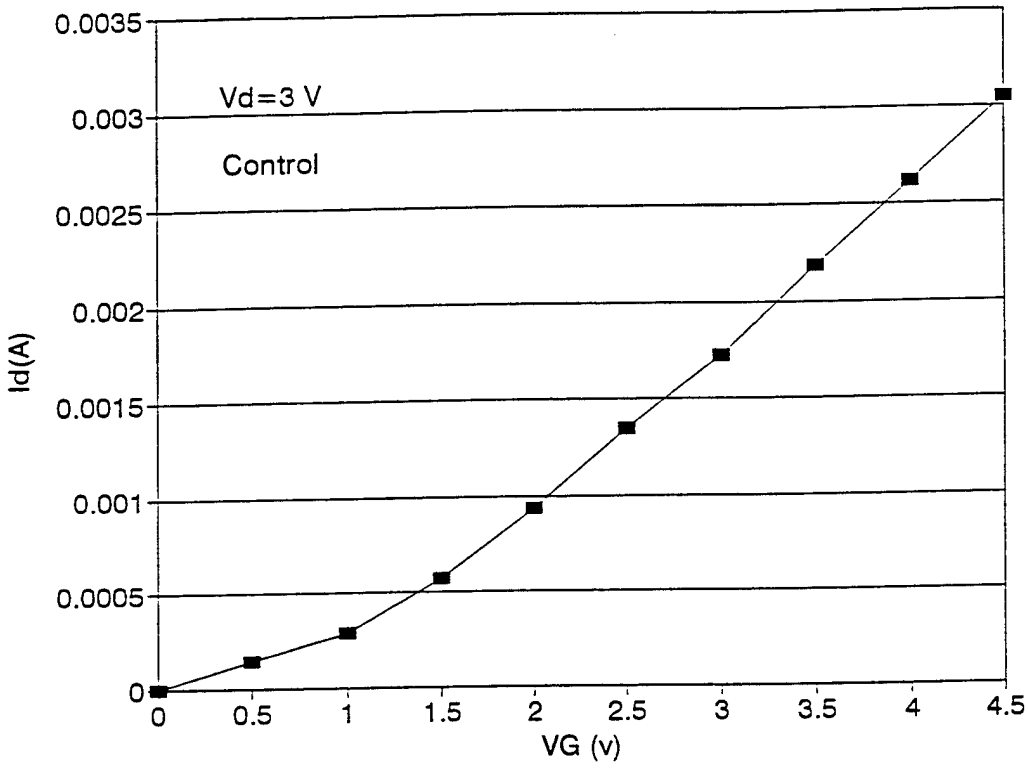


Fig. 4-7(b) I-V curves of control n-channel MOSFET. The channel length is 10μm, oxide thickness is 370Å.

4.2.5 Charge Trapping in Oxide

To determined the electron trapping properties of the oxide, an electron current of 1×10^{-7} A/cm^2 is injected through the oxide to induce electron trapping. The charge due to the trapped electrons in the oxide induces a flatband voltage shift. The amount of trapped charge is proportion to the flatband voltage shift (ΔV_f). Figure 4.8 shows the flatband voltage shift versus time curves for each sample. In these curves the trapping properties are dominated by traps with a large cross section. Each curve is a composite of three exponential curves. This indicates three different traps are involved. The cross section of these traps can be calculated. The details is described in appendix c. The cross sections and trap density for each sample is shown in table 4.1.

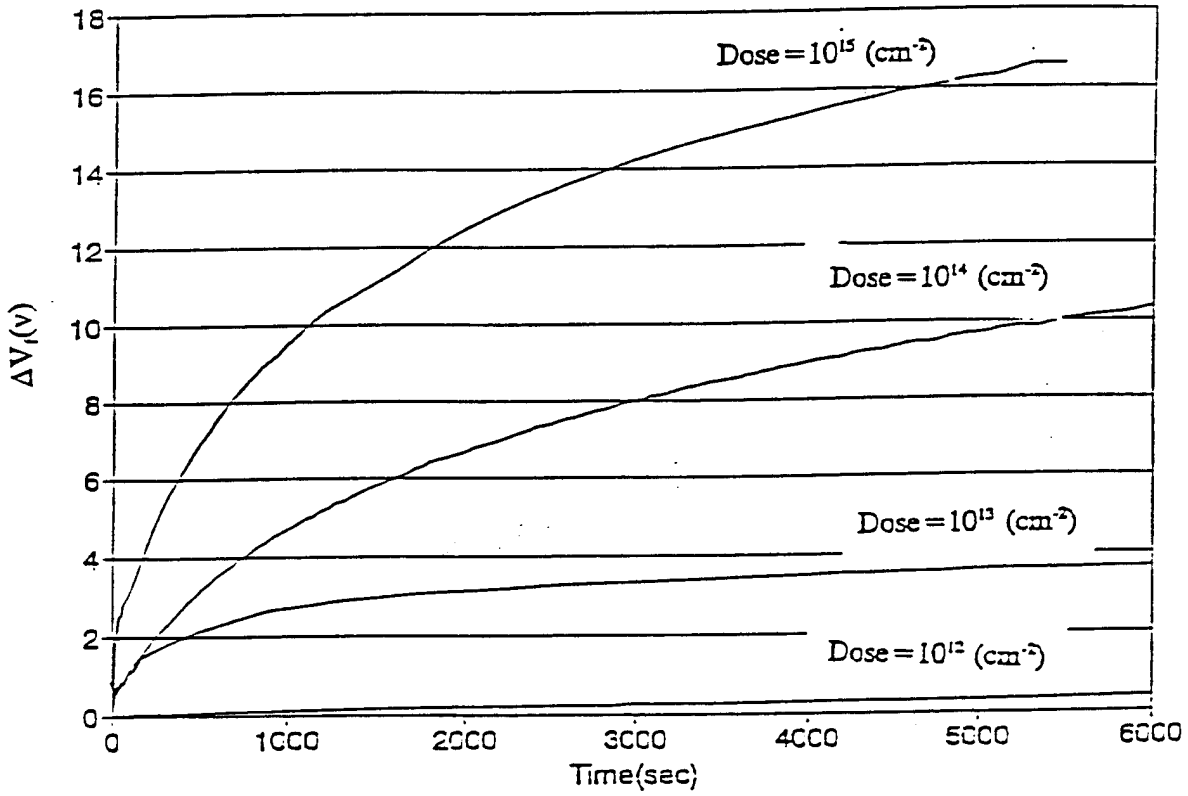


Fig 4.8 Flat band voltage shift(ΔV_f) versus injection time curves.

Dose(/cm^2)	Cross Section (cm^2)	Trap Density(cm^{-2})
10^{15}	$\sigma_1=5.0\times10^{-12}$	2.0×10^{12}
	$\sigma_2=1.5\times10^{-13}$	5.0×10^{12}
	$\sigma_3=3.0\times10^{-14}$	1.1×10^{13}
10^{14}	$\sigma_1=3.0\times10^{-13}$	2.0×10^{12}
	$\sigma_2=1.0\times10^{-14}$	5.0×10^{12}
	$\sigma_3=5.0\times10^{-15}$	8.0×10^{12}
10^{13}	$\sigma_1=3.0\times10^{-15}$	2.0×10^{12}
	$\sigma_2=4.1\times10^{-16}$	1.2×10^{12}
	$\sigma_3=1.5\times10^{-17}$	1.0×10^{12}
10^{12}	$\sigma_1=2.0\times10^{-16}$	6.0×10^{10}
	$\sigma_2=3.5\times10^{-17}$	1.7×10^{11}
	$\sigma_3=6.0\times10^{-18}$	8.0×10^{11}

Table 4.1 Oxide electron trap density calculated from figure 4.8.

From fig. 4.8 and table 4.1, we notice that the electron trap density increases with the germanium dose. This can be explained as follows: After a post implantation annealing treatment (PIA), some Ge remains in the SiO_2 and is incorporated in the oxide. The Ge in the SiO_2 is not incorporated in fully oxidized state (GeO_2) but more likely as

GeO. Ge bonds that are not involved in the network formation act as very efficient electron traps.

In this section we have presented the electrical properties of Ge implanted sample. The germanium implantation does reduce hot carrier injection in a MOS capacitor and the amount of hot carrier reduction depends on the dose of Ge. In order to prevent the increase of the interface state density, the implantation dose must be lower than $10^{13}/cm^2$. According to the above results, the optimum dose is 10^{13} $/cm^2$. In the oxide charge trapping study, we discover that the germanium in the SiO_2 increases the electron trapping rate. In the next section, we will propose a method to reduce this effect.

4.3 Oxide Charge Trapping Reduction

In section 4.2 we observe that the germanium implanted MOS, fabricated with the process described in chapter 3, has a large electron trapping rate. Because some of the germanium is in the oxide and forms GeO. F.K. LeGoues et al[95] found that the Ge was completely rejected from the oxide and piles up at the SiO_2/SiGe interface when they oxidized SiGe alloys. We are indebted to Professor Ralph Jaccodine who told us about this result. Their discovery could be the solution to our oxide charge trapping problem. If we implanted the Ge before oxidation, the Ge will be rejected from the oxide and the electrical properties of the oxide under this condition could be improved. In this section we will present the results of the MOS capacitors fabricated by the modified process procedure and compare them with the former results.

The electron trapping properties were compared between the original and modified techniques. Figure 4.9 shows their flatband voltage shift versus injection time curves measured by the avalanche injection technique. The correspondent charge trapping cross sections and electron tapping density are displayed in table 4.2. The cross section of the modified process is reduced and very close to that of control sample.

The hot carrier injection current of the modified Ge implanted MOS are shown in figure 4.10. The hot carrier reduction effect is reduced in the sample manufactured by modified technique.

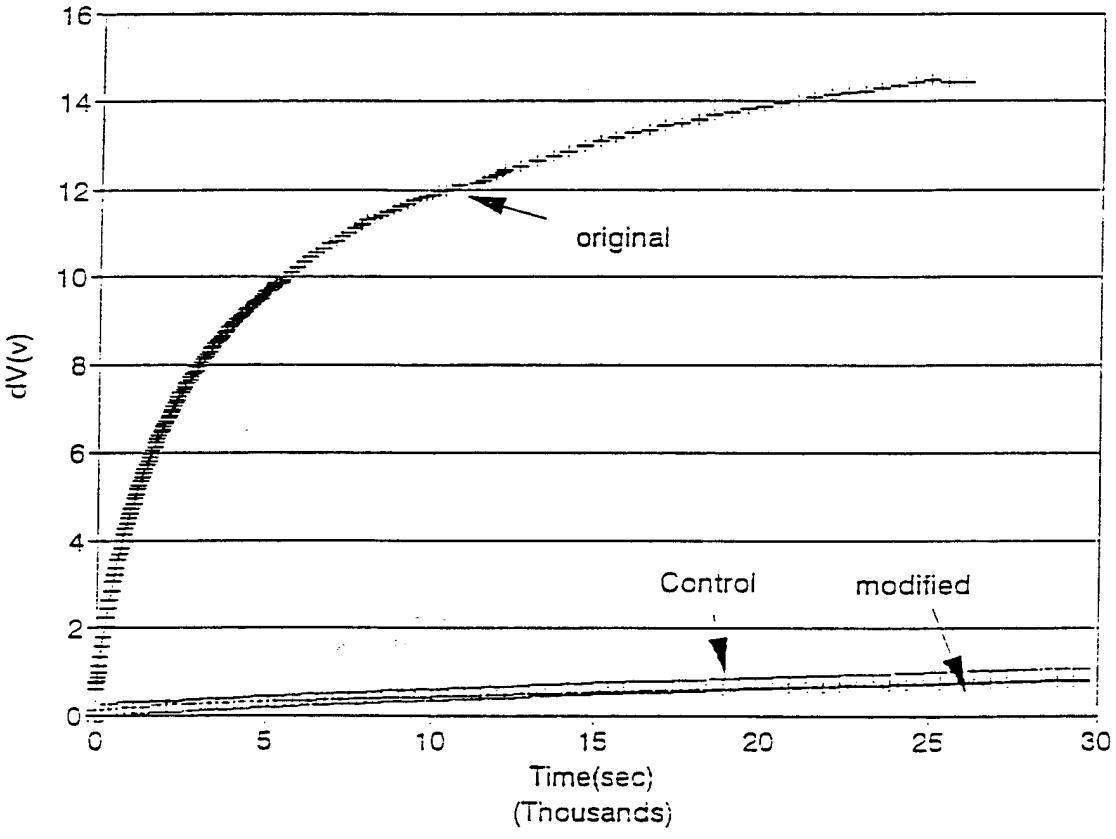


Fig. 4.9 Flatband voltage shift versus time curves for the samples fabricated by the original process "+" and the modified process "*" and control sample "□".

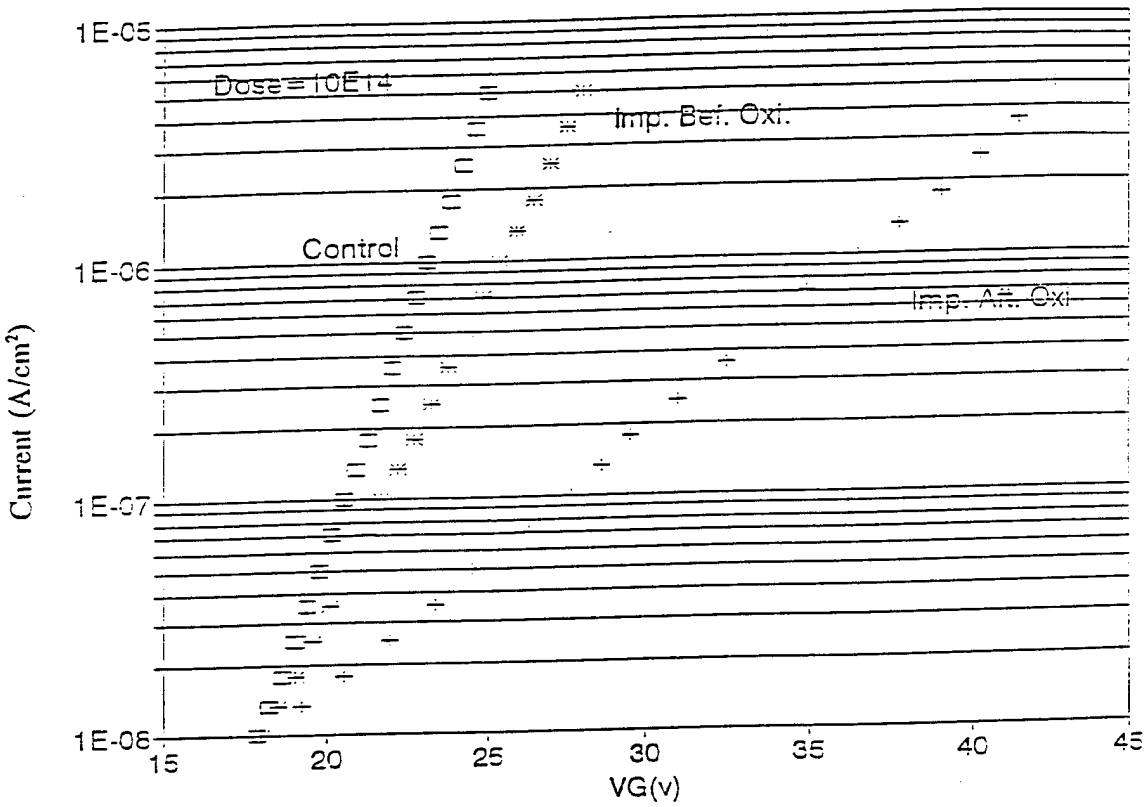


Fig. 4.10 Avalanche injection current versus Gate voltage curves. "+" is the sample fabricated by the original process, "*" is the sample fabricated by the modified process and "□" is the control sample.

The C-V curve of the sample is plotted in figure 4.11. We observed a larger stretch-out in the modified sample and the strong inversion capacitance increases. The interface state density of the sample is plotted in figure 4.12. The sample has a higher interface state density than the original sample.

Sample	Cross Section (cm^2)	Trapping Density(cm^{-2})
Original	$\sigma_1=3.0\times10^{-13}$	2.0×10^{12}
	$\sigma_2=1.0\times10^{-14}$	5.0×10^{12}
	$\sigma_3=5.0\times10^{-15}$	8.0×10^{12}
Modified	$\sigma_1=2.5\times10^{-16}$	5.0×10^{10}
	$\sigma_2=4.0\times10^{-17}$	2.0×10^{11}
	$\sigma_3=5.8\times10^{-18}$	7.5×10^{11}

Table 4.2 Oxide electron trapping cross section and trapping density calculated from figure 4.9.

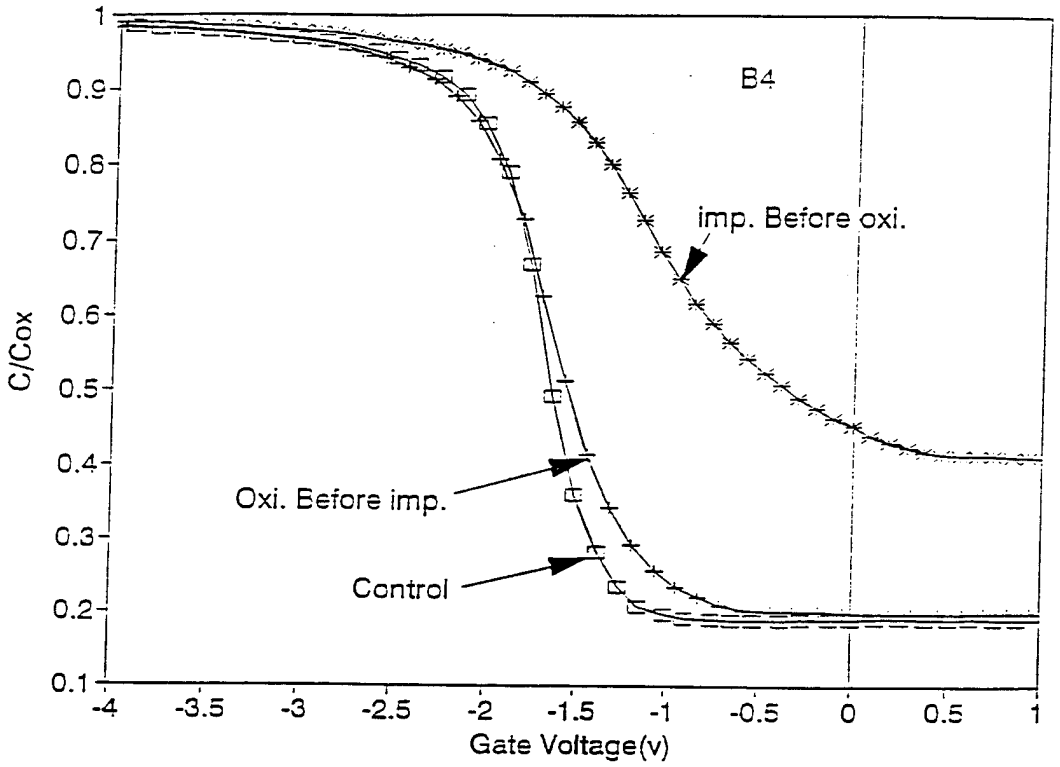


Fig. 4.11 High frequency C-V curves. "+" is the sample fabricated by the original process, "*" is the sample fabricated by the modified process and "□" is the control sample.

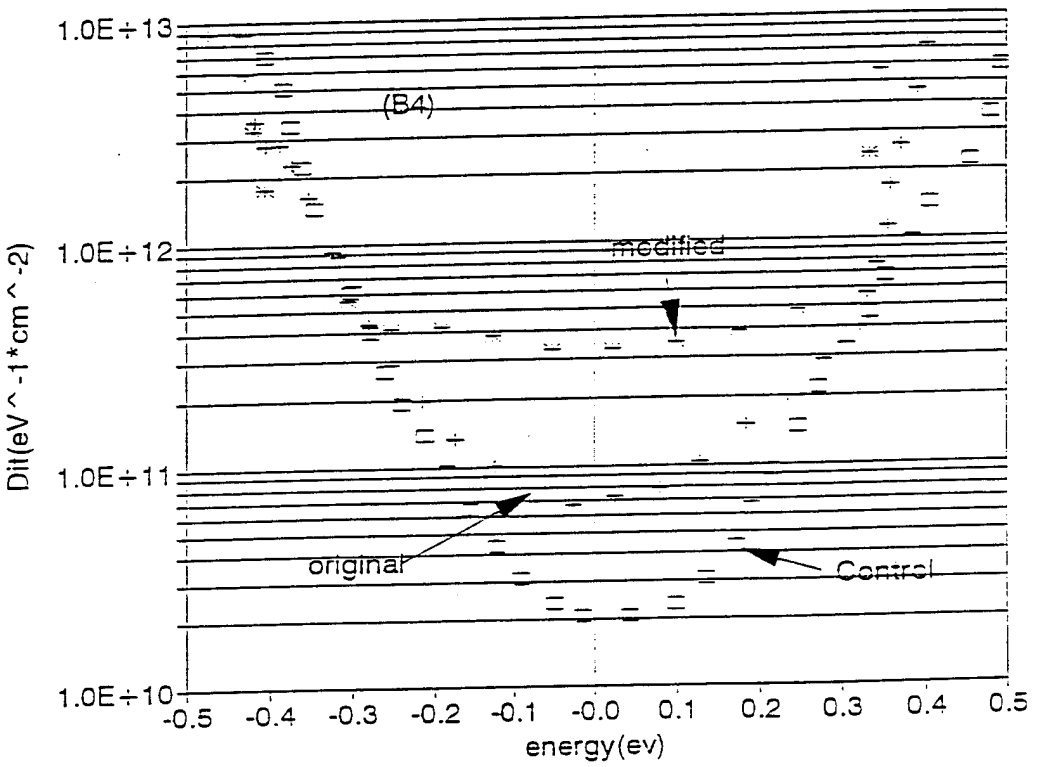


Fig. 4.12 The interface state densities versus energy curves. "+" is the sample fabricated by the original process, "*" is the sample fabricated by the modified process and "□" is the control sample.

From the results shown in this section, we realize that if we implant the Ge before oxidation. The Ge will be rejected from the oxide and reduces the electron trapping rate. However, the pile up of the Ge at the interface increases the interface state density and changes the effective doping at the interface. Additionally, the hot carrier reduction effect we observed in the original sample is reduced. This is because most of the Ge piles-up at the interface, the amount of Ge left in the bulk silicon is not enough to cause a large hot carrier reduction.

4.4 The effect of Ge Peak Position

In section 4.2, we determined the optimum dose by varying the dose at the same implantation energy. In this section, we will fix the dose at $10^{14}/cm^2$ and vary the energy to find out the optimum location of the peak concentration of germanium for the hot carrier reduction effect. Different energies (70, 80 and 90 KeV) were used to implante the germanium into the sample. The simulation profile of germanium is plotted in figure 4.13. Note that the correspond peak location is right at the interface for the 70KeV and moves into the Si substrate as the energy increases.

The hot carrier injection current and hot carrier energy curves of these sample are shown in figure 4.14 and 4.15. The hot carrier current increases with the implantation energy. The 70KeV sample has the largest hot carrier reduction. From this experiment, we know the optimum peak position for Ge implantation is at the Si-SiO_2 interface.

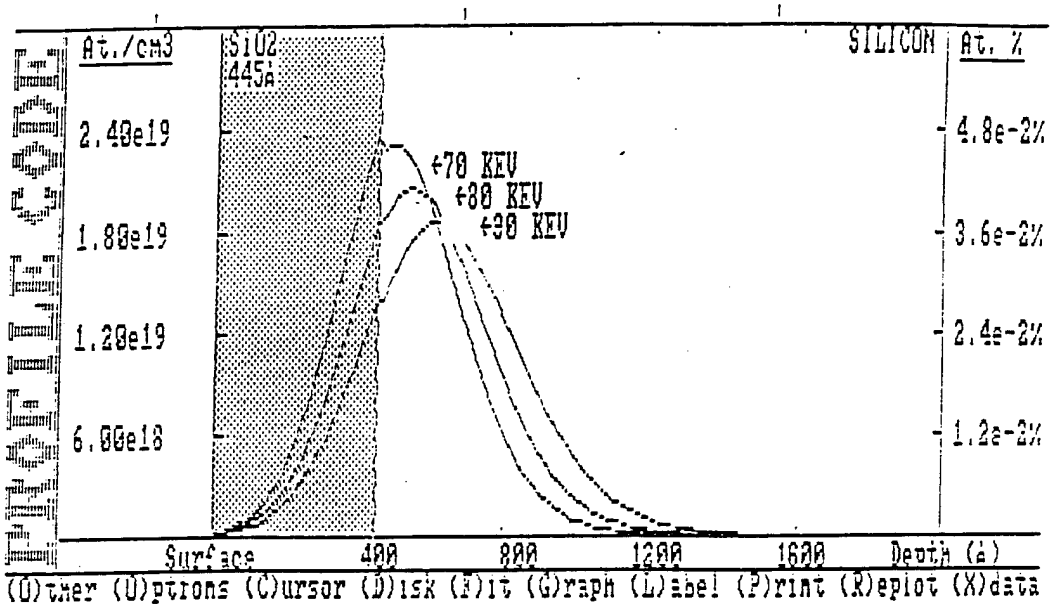


Fig.4.13 Simulation profiles of Ge in Si with implantation energy 70, 80 and 90 KeV.

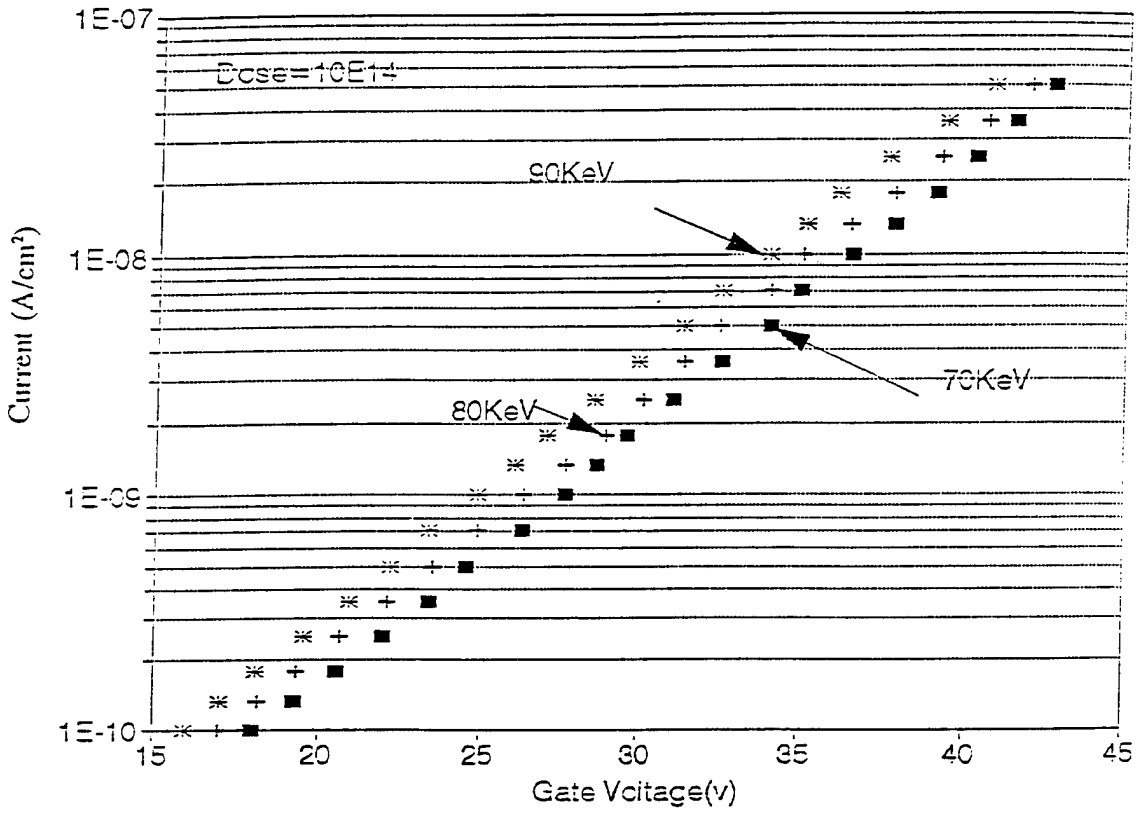


Fig. 4.14 Injection current versus Gate voltage curves for the samples implanted with different energy (70, 80, 90 KeV).

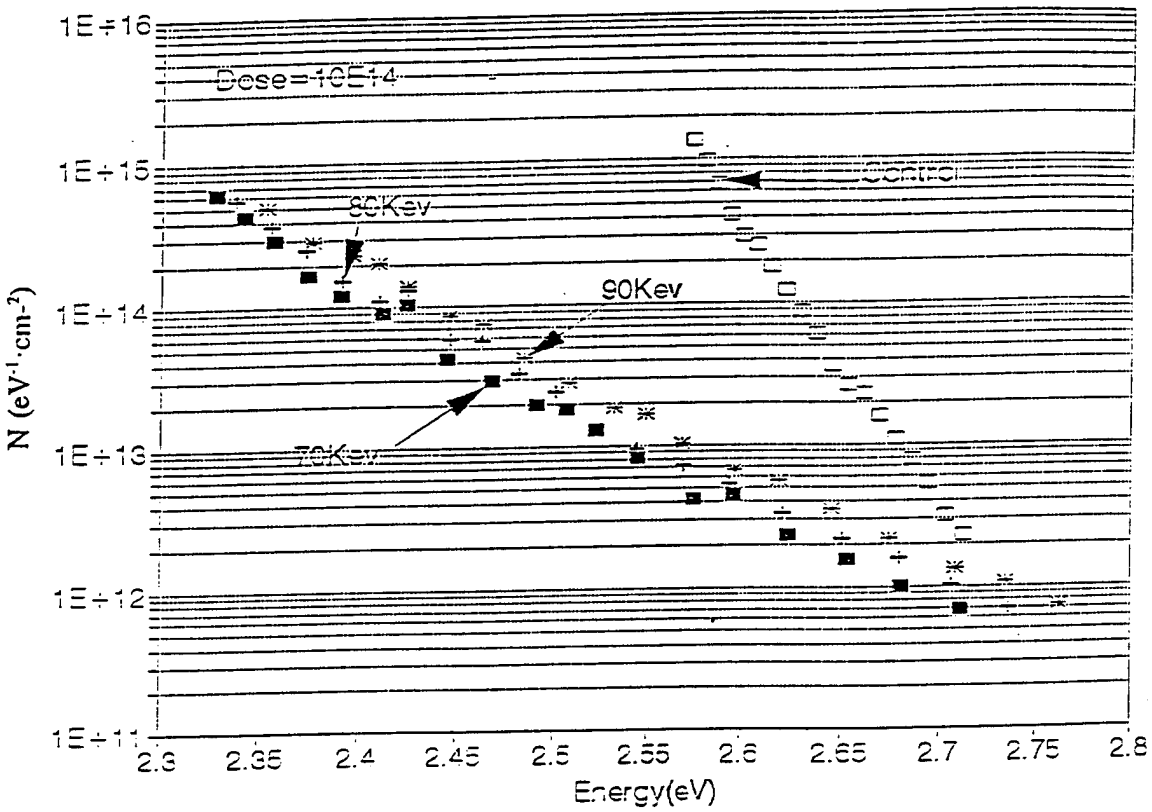


Fig. 4.15 Hot carrier energy distribution curves calculated from figure 4.14

4.5 Hot Carrier Effect at Liquid Nitrogen Temperature

There is considerable interest in operating devices at low temperatures to increase the current gain. One drawback of operating at low temperature is the increase in the hot carrier injection. At the low temperature, the scattering of the carriers in silicon is reduced, so the carriers are able to gain more energy from the applied field. The germanium implantation is one possible solution, because it introduces additional scattering for the hot carrier but does not change the current gain. We examines the hot carrier effect of the Ge implanted sample at liquid nitrogen temperature, the result is shown in figure 4.16. At liquid nitrogen temperature, the hot carrier injection current is strongly reduced. We also calculated the hot carrier energy distribution curve and plotted in figure 4.17. Note the hot carrier energy density is reduced under this condition.

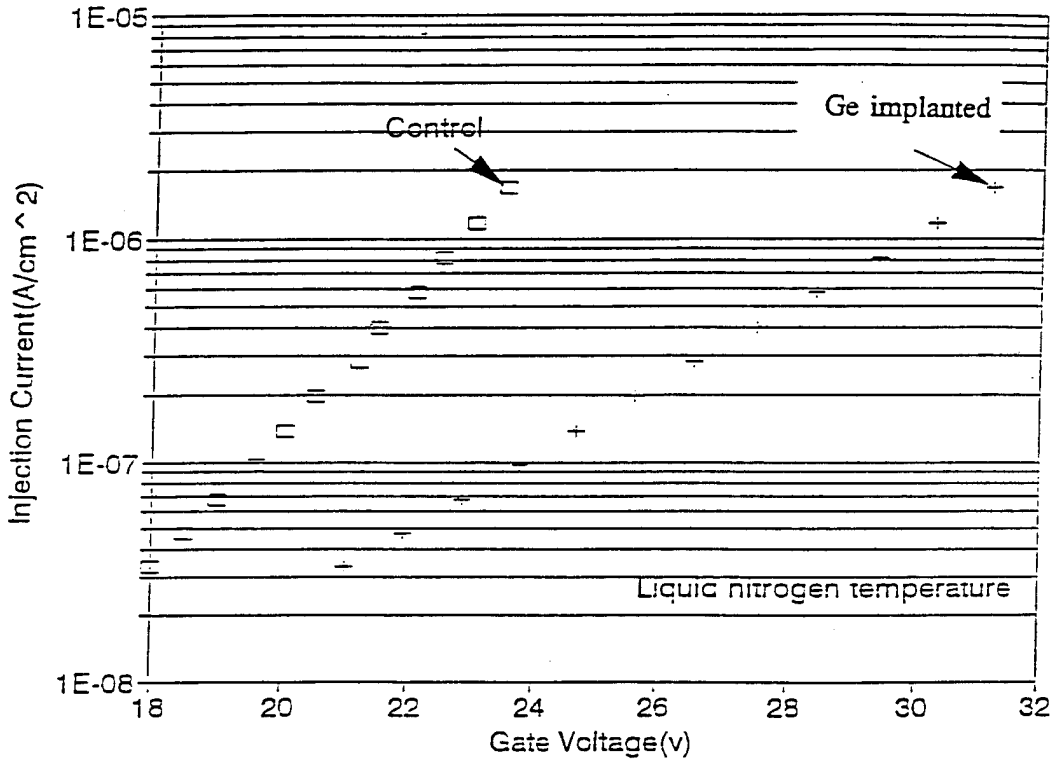


Fig. 4.16 Aalanche current versus Gate voltage curve of Ge implanted sample measured at liquid nitrogen temperature.

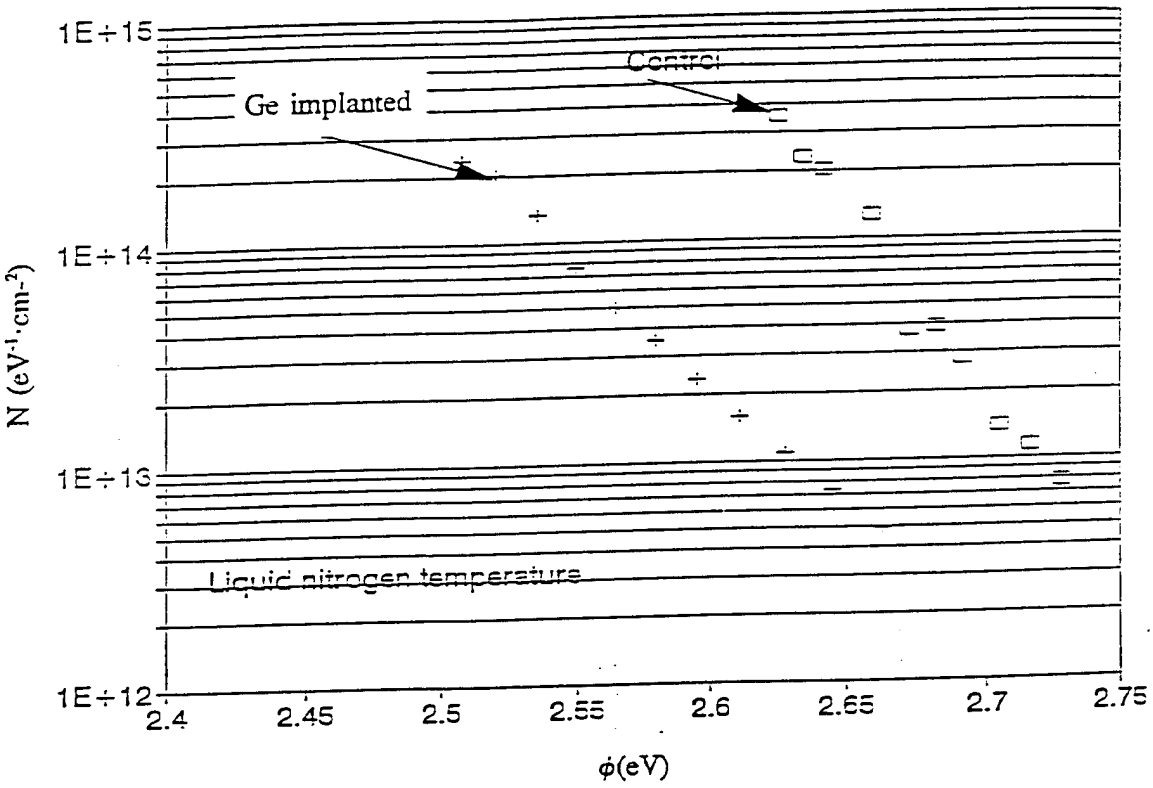


Fig. 4.17 Hot carrier energy distribution calculated from Fig. 4.16.

4.6 Carbon Implanted Sample

We also study the effect of carbon on the MOS electrical properties. The C-V curves of the C implanted and Ge implanted MOS capacitors are plotted in figure 4.18. The C implantation introduces more interface states than Ge implantation as shown by the larger stretch-out is observed in the C-V curve of the C implanted sample. The hot carrier injection current curve of the C implanted sample is shown in figure 4.19 and the hot carrier energy curve is plotted in figure 4.20. We did not observe any hot carrier reduction effect as was observed for the Ge sample.

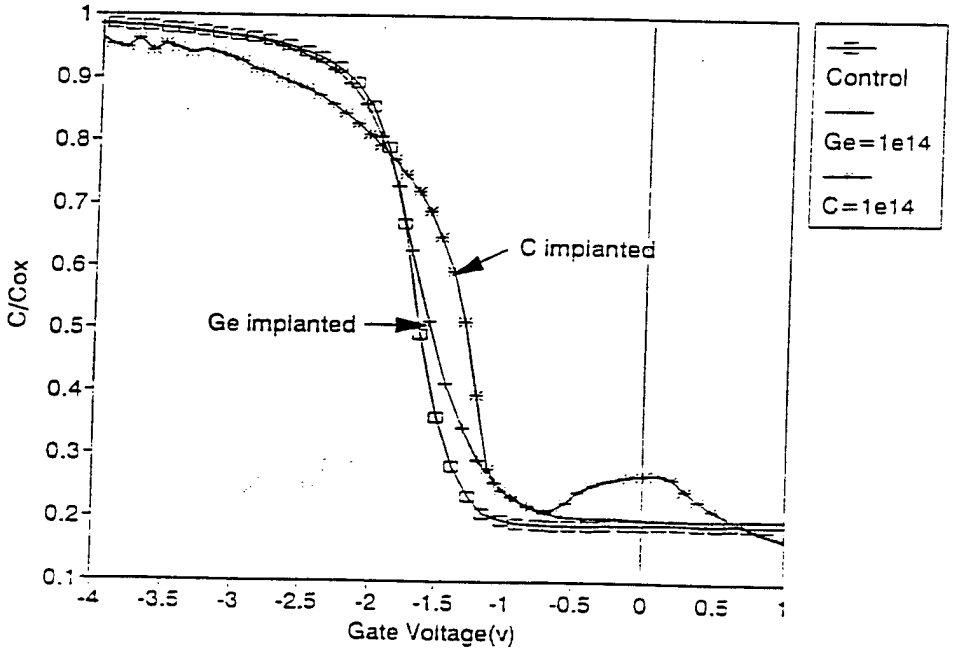


Fig. 4.18 The high frequency C-V curves of C implanted "*" , Ge implanted "+" and control "□" samples. The dose are $10^{14}/cm^2$ for both implanted samples.

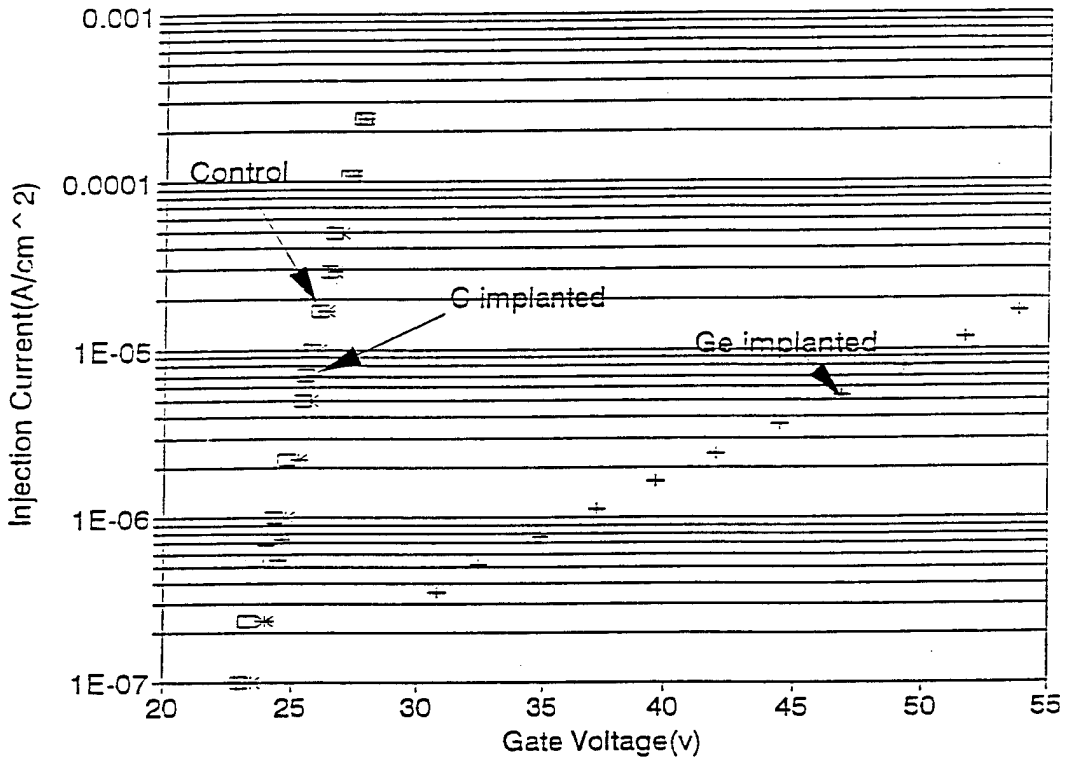


Fig. 4.19 Avalanche injection current against gate voltage curves for the C "*" and Ge "+" implanted and control "□" samples.

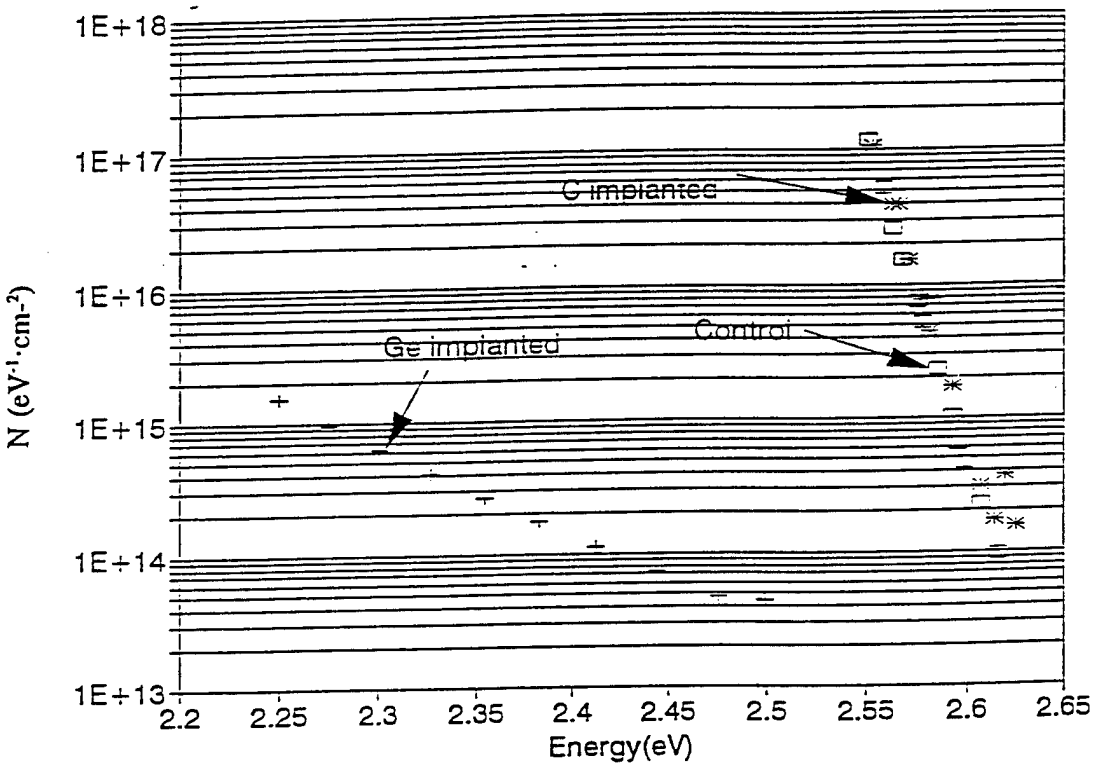


Fig. 4.20 The hot carrier energy distribution curves of the C and Ge implanted samples calculated from figure 4.19.

Chapter 5 Conclusions

5.1 Introduction

The contributions of this dissertation will be briefly stated in this chapter. First, we studied the effects of Ge implantation on the MOS devices and optimized the Ge implantation technique. Secondly, we proposed an accurate method to evaluate the Si-SiO_2 interface state density using an improved Q-V technique. Finally we will recommend some directions for future research.

5.2 Effects of Ge Implantation

The experimental results of avalanche injection show that the population of hot carriers in the Si is strongly reduced by the Ge implantation. In the interface state density study, we found that when the Ge dose is equal to than $10^{14}/cm^2$ the interface state density increases. To obtain the maximum hot carrier reduction without increasing the interface state density, the implantation dose must be less than $10^{14}/cm^2$. The effect of Ge peak location on the hot carrier injection has been studied, the optimum peak location is at the Si-SiO_2 interface.

The oxide charge trapping study showed that the trapping rate of the Ge implanted samples in the SiO_2 increases with the Ge dose. We believe that the increase in trapping rate results from the formation of GeO. Because the Ge bonds that are not involved in the network formation act as very efficient electron traps. Since this phenomena is caused by the Ge in the SiO_2 , We have proposed a modified method that rejects Ge

from the oxide. In the modified process, We implanted Ge before oxidation. The experimental results show that the oxide charge trapping cross section of the sample made by the modified method is reduced but the hot carrier reduction effect is also reduced. Additionally the interface state density of the new samples increases. During the oxidation, the Ge piles up at the Si-SiO_2 interface, the Ge concentration is reduced in both the SiO_2 and the Si. Thus, reduction in hot electron injection is reduced. The effect of Ge implantation on the hot carrier injection at liquid nitrogen temperature has been presented. The Ge also reduces the injection at this temperature. The effects of carbon implantation have also been presented. We did not observe a hot carrier reduction effect in the C implanted sample. The C implanted samples have larger interface state density than the Ge implanted sample.

5.3 Q-V Technique

A new approach to the interface state density using Q-V measurement is introduced in chapter three. This technique provides a direct and accurate method to evaluate the Si-SiO_2 interface. A major advantage of the Q-V technique as compared with other techniques is that it does not depend on the semiconductor doping concentration. Frequently, this concentration is not accurately known and it is a major concern in practical cases when the concentration changes with depth in the silicon substrate. The computerized Q-V measurement system has been successfully developed in our laboratory and used to evaluate our Ge implanted samples. We have developed a new technique to determine the unknown constant that is independent of the silicon

doping.

5.4 Suggestion for Future Studies

The characterization and optimization of Ge implantation technique has been achieved in this dissertation. Several suggestions will be given for the future studies in this area.

(1) Although the method used in section 4.3 does improve the oxide charge trapping rate, it also decreases the hot carrier reduction effect of Ge implanted samples. A new approach has to be used to improve the oxide charge trapping property without affecting the hot carrier reduction effect of the Ge implanted samples. The possible solution is to find a suitable annealing treatment to reduce charge trapping center.

(2) In this dissertation, the MOSFET structure is only used to study the effect of Ge on mobility. The hot carrier injection of MOSFET devices has not been measured. In the future the MOSFET hot carrier injection should be studied.

(3) The results obtained in this dissertation can be used in short channel MOSFET's to reduce the hot carrier effect. This needs to be investigated.

Appendix A

Fabrication Sequence for MOS Capacitor

1. Starting Material

- □ 2-inch wafer, p-type $<100>$, $0.1 \sim 0.2$ Ω-cm

2. Oxidation

- □ RCA clean
- □ oxidation: 1000°C, 45 minutes, dry oxide, 450Å
- □ anneal: 1000°C, 15 minutes, 1.5 l/min N_2

3. Ge implantation

- □ implantation: Ge, 70 KeV, 10^{12}, 10^{13}, 10^{14}, 10^{15} cm^{-2}
- □ post implant anneal: 950°C, 30 min, 1.5 l/min N_2

4. Metallization

- □ Al deposition: evaporator
- □ photo: define gate area
- □ etch Al: PAN etch, 45°C, 3 minutes
- □ strip PR: PRS-2000
- □ anneal: PMA, 450°C, forming gas(H_2/N_2, 1:5)

Appendix B

Fabrication Sequence for the N-Channel MOSFET

1. Starting Material

- □ 3-inch, p-type<100> Si, 1~2 Ω-cm

2. LOCOS Oxidation

- □ RCA clean
- □ pad oxide: 950°C, 12 min, wet O_2, 300Å
- □ nitride: LPCVD, 750°C, 35minutes, 0.3 Torr, NH_3:$SiCl_2H_2$, 1200Å
- □ photo: define the active area
- □ plasma etch nitride: o.3 Torr, 125 W, CF_4, 2 min

3. Field Implant

- □ fron implant: BF_2, 145 KeV, 5×10^{14} cm^{-2}
- □ back implant: B, 32 KeV, 2×10^{15} cm^{-2}
- □ strip PR: PRS-2000
- □ anneal: 950°C, 30 min, N_2
- □ etch oxide: BHF, 1 min

4. Field Oxide

- □ RCA clean
- □ oxide: 1100°C, 70 min, wet O_2, 6kÅ
- □ etch oxide: BHF, 2 min

- ☐ etch nitride: H_3PO_4, 165°C, 1 hour
- ☐ etch oxide: BHF until hydrophobic

5. Sacrifice Oxide

- ☐ RCA clean
- ☐ oxide: 950°C, 12 min, wet O_2, 300Å
- ☐ etch oxide: BHF until hydrophobic

6. Ge Implantation

- ☐ Ion Implantation: Ge, 10^{14} cm^{-2}, 30 KeV
- ☐ anneal: 950°C, 30 min, N_2

7. Gate Oxide

- ☐ RCA clean
- ☐ oxide: 950°C, 105 min, 1.5 l/min O_2, 370Å
- ☐ anneal: 950°C, 30 min, 1.5 l/min, N_2, *in situ*

8. Polysilicon gate

- ☐ LPCVD: 0.8 Torr, 280 sccm SiH_4, 625°C, 30 min, 5 kÅ
- ☐ photo: polygate definition
- ☐ plasma etch: poly, 0.3 Torr, 200 W, SF_6, 5 min
- ☐ strip PR: PRS-2000
- ☐ RCA clean
- ☐ diffusion: $POCl_3$, 900°C, 20 min
- ☐ drive in: N_2, 900°C, 30 min
- ☐ etch p-glass: BHF, 15 sec

9. Contact Window

- ☐ RCA clean
- ☐ oxide: 900°C, 45 min, wet O_2, 1200Å
- ☐ photo: define the contact window
- ☐ etch oxide: BHF, 4 min
- ☐ strip PR: PRS-2000

10. Metallization

- ☐ RCA clean + HF dip
- ☐ Al sputtering: front side, 7kÅ, 7Hg, 0.4Amp
- ☐ photo: connection
- ☐ etch Al: PAN etch, 45°C, 2min
- ☐ strip PR: PRS-2000

Appendix C

Exponential Fitting of Oxide Traps

Experimental results indicate that several different traps are involved. The total voltage shift can be expressed by the summation of n different traps as follows

$$\Delta V=\sum_{i=1}^{n} \Delta V_{fi}\left[1-\exp\left(-\frac{t}{\tau_i}\right)\right] \qquad \text{(C1)}$$

Take the derivative with respect to time t on both sides of the above equation gives the following expression,

$$\frac{d\Delta V}{dt}=\sum_{i=1}^{n} \frac{\Delta V_{fi}}{\tau_i}\exp\left(-\frac{t}{\tau_i}\right) \qquad \text{(C2)}$$

If we consider one of these traps, the *ith* trap and take the logarithm of both sides of the equation we obtain

$$\ln\frac{d\Delta V_i}{dt}=\ln\frac{\Delta V_{fi}}{\tau_i}-\frac{t}{\tau_i} \qquad \text{(C3)}$$

As a result we can see that a plot of $\ln(d\Delta V_i/dt)$ vs t should be linear. Two useful parameters, τ_i and ΔV_{fi}, can be determined by the slope and intercept of the above linear plot, $\ln(d\Delta V_i/dt)$ versus t. The trap cross section and density can be calculated using equations (3.14) and (3.15).

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